

EXHIBIT A

TOWNSEND AND TOWNSEND AND CREW LLP
ERIC P. JACOBS (State Bar No. 88413)
PETER H. GOLDSMITH (State Bar No. 91294)
ROBERT A. McFARLANE (State Bar No. 172650)
IGOR SHOIKET (State Bar No. 190066)
Two Embarcadero Center, 8th Floor
San Francisco, California 94111
Telephone: (415) 576-0200
Facsimile: (415) 576-0300
E-mail: epjacobs@townsend.com
phgoldsmith@townsend.com
ramcfarlane@townsend.com
ishoiket@townsend.com

Attorneys for Defendant
FAIRCHILD SEMICONDUCTOR CORPORATION

UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR,
INC., a California corporation; and
ALPHA & OMEGA SEMICONDUCTOR,
LTD., a Bermuda corporation,

Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR
CORP., a Delaware corporation,
Defendant and Counterclaimant.

Case No. C 07-2638 JSW
(Consolidated with Case No. C 07-2664 JSW)

**ANSWER TO COMPLAINT FOR
PATENT INFRINGEMENT AND
DECLARATORY JUDGMENT; FIRST
AMENDED COUNTERCLAIMS FOR
PATENT INFRINGEMENT AND
DECLARATORY JUDGMENT**

JURY TRIAL DEMANDED

AND RELATED COUNTERCLAIMS.

Defendant Fairchild Semiconductor Corporation ("Fairchild"), by and through its attorneys, hereby answers the Complaint for Patent Infringement and Declaratory Judgment ("Complaint") of plaintiffs Alpha & Omega Semiconductor, Ltd., ("AOS, Ltd.") and Alpha & Omega Semiconductor, Inc., ("AOS, Inc.") (collectively, "AOS") as follows:

PARTIES

1. Fairchild is without sufficient knowledge or information to form a belief as to the truth or falsity of the allegations of paragraph 1 of the Complaint, and denies them on such basis.

2. Fairchild is without sufficient knowledge or information to form a belief as to the truth or falsity of the allegations of paragraph 2 of the Complaint, and denies them on such basis.

3. Fairchild admits that it is a Delaware corporation, with a place of business at 82 Running Hill Road, South Portland, ME 04106.

JURISDICTION AND VENUE

4. Fairchild admits that the Complaint purports to assert claims arising under the patent laws of the United States, 35 U.S.C. §§ 1 *et seq.* and the Declaratory Judgment Act, 28 U.S.C. §§ 2201 and 2202. Fairchild also admits this Court has subject matter jurisdiction over this action under 28 U.S.C. §§ Section 1331 and 1338(a). Except as so admitted, Fairchild denies the remaining allegations of paragraph 4 of the Complaint.

5. Fairchild admits that this Court has personal jurisdiction over Fairchild and that it has facilities located in San Jose, California. Fairchild admits that it has communicated with AOS in California regarding AOS's business and Fairchild's patents. Except as so admitted, Fairchild denies the remaining allegations of paragraph 5 of the Complaint.

6. Fairchild admits that venue is proper in this judicial district.

INTRADISTRICT ASSIGNMENT

7. Fairchild admits that this action is subject to assignment on a district-wide basis under the local rules of this Court.

GENERAL ALLEGATIONS

8. Fairchild is without sufficient knowledge or information to form a belief as to the truth or falsity of the allegations of paragraph 8 of the Complaint, and denies them on such basis.

9. Fairchild admits that the face of U.S. Patent No. 5,907,776 ("the '776 patent"), entitled "Method of Forming a Semiconductor Structure Having Reduced Threshold Voltage and High Punch-through Tolerance," states that it was issued on May 25, 1999. Fairchild also admits that the face of U.S. Patent No. 5,767,567 ("the '567 patent"), entitled "Design of Device Layout for Integration with

1 Power MOSFET Packaging to Achieve Better Lead Wire Connections and Lower On Resistance,"
 2 states that it was issued on June 16, 1998. Except as so admitted, Fairchild is without sufficient
 3 knowledge or information to form a belief as to the truth or falsity of the remaining allegations of
 4 paragraph 9 of the Complaint, and denies them on such basis.

5 10. Fairchild is without sufficient knowledge or information to form a belief as to the truth
 6 or falsity of the allegations of paragraph 10 of the Complaint, and denies them on such basis.

7 11. Fairchild admits that it has alleged that AOS infringes U.S. Patent No. 6,429,481 ("the
 8 '481 patent"), entitled "Field Effect Transistor and Method of its Manufacture," and U.S. Patent No.
 9 6,710,406 ("the '406 patent"), entitled "Field Effect Transistor and Method of its Manufacture," and
 10 that these patents issued on August 6, 2002, and March 23, 2004, respectively.

11 12. Fairchild admits that it has directed correspondence to AOS stating that certain AOS
 12 products infringe the '481 and '406 patents and requesting that AOS license rights to those patents.
 13 Fairchild is without sufficient knowledge or information to form a belief as to the truth or falsity of the
 14 remaining allegations of paragraph 12 of the Complaint, and denies them on such basis.

15 13. Fairchild is without sufficient knowledge or information to form a belief as to the truth
 16 or falsity of the allegations of paragraph 13 of the Complaint, and denies them on such basis.

17 14. Fairchild admits that AOS's complaint denies that AOS infringes any valid and
 18 enforceable claim of any of the Fairchild patents, but Fairchild denies the basis for AOS's denial.

19 15. Fairchild admits that an actual and justiciable controversy exists between Fairchild and
 20 AOS concerning whether AOS infringes any valid claim of the '481 and '406 patents and that AOS's
 21 Complaint seeks a declaratory judgment that the claims of the '481 and '406 patents are invalid and
 22 that AOS does not infringe any valid claim of certain of the '481 and '406 patents.

23 **FIRST CLAIM FOR RELIEF**
 24 **(Alleged Infringement of U.S. Patent No. 5,907,776 by Fairchild)**

25 16. Fairchild incorporates herein by reference its responses to paragraphs 1 through 10 of
 26 the Complaint.

27 17. Fairchild denies each and every allegation of paragraph 17 of the Complaint.

28 18. Fairchild denies each and every allegation of paragraph 18 of the Complaint.

19. Fairchild denies each and every allegation of paragraph 19 of the Complaint.

20. Fairchild denies each and every allegation of paragraph 20 of the Complaint.

SECOND CLAIM FOR RELIEF
(Alleged Infringement of U.S. Patent No. 5,767,567 by Fairchild)

21. Fairchild incorporates herein by reference its responses to paragraphs 1 through 10 of the Complaint.

22. Fairchild denies each and every allegation of paragraph 22 of the Complaint.

23. Fairchild denies each and every allegation of paragraph 23 of the Complaint.

24. Fairchild denies each and every allegation of paragraph 24 of the Complaint.

25. Fairchild denies each and every allegation of paragraph 25 of the Complaint.

THIRD CLAIM FOR RELIEF
(Alleged Non-Infringement of U.S. Patent No. 6,429,481)

26. Fairchild incorporates herein by reference its responses to paragraphs 1 through 15 of the Complaint.

27. Fairchild denies each and every allegation of paragraph 27 of the Complaint.

FOURTH CLAIM FOR RELIEF
(Alleged Non-Infringement of U.S. Patent No. 6,710,406)

28. Fairchild incorporates herein by reference its responses to paragraphs 1 through 15 of the Complaint.

29. Fairchild denies each and every allegation of paragraph 29 of the Complaint.

AFFIRMATIVE DEFENSES

Fairchild, for its further and separate defenses to the allegations of the Complaint, alleges as follows:

FIRST AFFIRMATIVE DEFENSE

1. The Complaint fails to state a claim upon which relief can be granted.

SECOND AFFIRMATIVE DEFENSE

2. Each claim of the '776 and the '567 patent is invalid for failure to meet one or more of

the conditions of patentability specified in Title 35 of the United States Code, including but not limited to 35 U.S.C. §§ 102, 103, 112, and/or 115.

THIRD AFFIRMATIVE DEFENSE

3. AOS's claim for relief is barred by the doctrine of prosecution history estoppel.

FOURTH AFFIRMATIVE DEFENSE

4. AOS's claim for damages is barred, in whole or in part, by the operation of applicable statutes, including 35 U.S.C. § 287.

FIFTH AFFIRMATIVE DEFENSE

5. AOS's claim for relief is barred by the doctrine of equitable estoppel

SIXTH AFFIRMATIVE DEFENSE

6. AOS's claim for relief is barred by the doctrine of laches.

COUNTERCLAIMS FOR DECLARATORY JUDGMENT

JURISDICTION AND VENUE

1. These counterclaims are brought under the patent laws of the United States, Title 35 of the United States Code. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 (Federal Question), 1338(a) (Patents), 2201 (Declaratory Relief), and 2202 (Declaratory Relief).

2. Venue is proper in this judicial district under 28 U.S.C. §§ 1391 and 1400.

3. This court has personal jurisdiction over AOS because AOS has availed itself of the jurisdiction of the Court by filing its Complaint. AOS also has sufficient minimum contacts with this State, maintains offices within this State and, on information and belief, conducts substantial business within this State.

PARTIES

4. Fairchild Semiconductor Corporation is a corporation duly organized and existing under the laws of the State of Delaware and has a place of business in San Jose, California.

5. On information and belief, Alpha and Omega Semiconductor Incorporated is a corporation organized and existing under the laws of the State of California and has a place of

business in Sunnyvale, California. On information and belief, Alpha and Omega Semiconductor Limited is a Bermuda corporation with a place of business in Taipei, Taiwan.

FIRST COUNTERCLAIM
(Declaratory Judgment of Non-Infringement)

6. Fairchild incorporates by reference the allegations of Paragraphs 1 through 5, as if fully set forth herein.

7. AOS purports to be the owner by assignment of the '776 and '567 patents.

8. An actual and justiciable case or controversy exists between Fairchild, on the one hand, and AOS, on the other hand, as to Fairchild's alleged infringement of the '776 and '567 patents by virtue of the allegations in the Complaint in this action.

9. Fairchild has not willfully or otherwise infringed, contributed to the infringement of, or actively induced others to infringe, and does not willfully or otherwise infringe, contribute to the infringement of, or actively induce others to infringe, any valid claim of the '776 and '567 patents.

10. Fairchild seeks a judicial determination from this Court that it has not willfully or otherwise infringed, contributed to the infringement of, or actively induced others to infringe, and does not willfully or otherwise infringe, contribute to the infringement of, or actively induce others to infringe, any valid claim of the '776 and '567 patents.

SECOND COUNTERCLAIM
(Declaratory Judgment of Invalidity)

11. Fairchild incorporates by reference the allegations of paragraphs 1 through 9, as if fully set forth herein.

12. An actual and justiciable case or controversy exists between Fairchild, on the one hand, and AOS, on the other hand, as to the validity of the claims of the '776 and '567 patents by virtue of the allegations in the Complaint in this action.

13. Each claim of the '776 and '567 patents is invalid for failure to meet one or more of the conditions of patentability specified in Title 35 of the United States Code, including but not limited to 35 U.S.C. §§ 101, 102, 103, and/or 112.

1 14. Fairchild seeks a judicial determination from this Court that the claims of the '776 and
2 '567 patents are invalid.

3 **THIRD COUNTERCLAIM**
4 **(Infringement of U.S. Patent No. 6,429,481)**

5 15. Fairchild incorporates by reference and realleges paragraphs 1 through 5.

6 16. On August 6, 2002, United States Patent No. 6,429,481 ("the '481 patent"), entitled
7 "Field Effect Transistor and Method of its Manufacture," was duly and legally issued by the United
8 States Patent and Trademark Office. Fairchild is the assignee of the '481 patent and continues to hold
9 all rights and interest in the '481 patent. A true and correct copy of the '481 patent is attached hereto
10 as Exhibit A.

11 17. AOS has directly, indirectly, contributorily, and/or by inducement infringed and
12 continues to infringe the '481 patent by its manufacture, use, sale, importation, and/or offer for sale of
13 certain products, including without limitation, AOS power transistors. AOS is liable for its
14 infringement of the '481 patent pursuant to 35 U.S.C. § 271.

15 18. AOS's acts of infringement have caused damage to Fairchild, and Fairchild is entitled
16 to recover from AOS the damages sustained as a result of AOS's wrongful acts in an amount subject to
17 proof at trial. AOS's infringement of Fairchild's exclusive rights under the '481 patent will continue to
18 cause damage to Fairchild, causing irreparable harm for which there is no adequate remedy at law
19 unless enjoined by this Court.

20 19. Upon information and belief, AOS's infringement of the '481 patent is willful and
21 deliberate, entitling Fairchild to increased damages under 35 U.S.C. § 284 and to attorneys' fees and
22 costs incurred in prosecuting this action under 35 U.S.C. § 285.

23 **FOURTH COUNTERCLAIM**
24 **(Infringement of U.S. Patent No. 6,710,406)**

25 20. Fairchild incorporates by reference and realleges paragraphs 1 through 5.

26 21. On March 23, 2004, United States Patent No. 6,710,406 ("the '406 patent"), entitled
27 "Field Effect Transistor and Method of its Manufacture," was duly and legally issued by the United
28 States Patent and Trademark Office. Fairchild is the assignee of the '406 patent and continues to hold

1 all rights and interest in the '406 patent. A true and correct copy of the '406 patent is attached hereto
2 as Exhibit B.

3 22. AOS has directly, indirectly, contributorily, and/or by inducement infringed and
4 continues to infringe the '406 patent by its manufacture, use, sale, importation, and/or offer for sale of
5 certain products, including without limitation, AOS power transistors. AOS is liable for its
6 infringement of the '406 patent pursuant to 35 U.S.C. § 271.

7 23. AOS's acts of infringement have caused damage to Fairchild, and Fairchild is entitled
8 to recover from AOS the damages sustained as a result of AOS's wrongful acts in an amount subject to
9 proof at trial. AOS's infringement of Fairchild's exclusive rights under the '406 patent will continue to
10 cause damage to Fairchild, causing irreparable harm for which there is no adequate remedy at law
11 unless enjoined by this Court.

12 24. Upon information and belief, AOS's infringement of the '406 patent is willful and
13 deliberate, entitling Fairchild to increased damages under 35 U.S.C. § 284 and to attorneys' fees and
14 costs incurred in prosecuting this action under 35 U.S.C. § 285.

15 **FIFTH COUNTERCLAIM**
16 **(Infringement of U.S. Patent No. 6,521,497)**

17 25. Fairchild incorporates by reference and realleges paragraphs 1 through 5.

18 26. On February 18, 2003, United States Patent No. 6,521,497 ("the '497 patent"), entitled
19 "Method of Manufacturing a Field Effect Transistor," was duly and legally issued by the United States
20 Patent and Trademark Office. Fairchild is the assignee of the '497 patent and continues to hold all
21 rights and interest in the '497 patent. A true and correct copy of the '497 patent is attached hereto as
22 Exhibit C.

23 27. AOS has directly, indirectly, contributorily, and/or by inducement infringed and
24 continues to infringe the '497 patent by its manufacture, use, sale, importation, and/or offer for sale of
25 certain products, including without limitation, AOS power transistors. AOS is liable for its
26 infringement of the '497 patent pursuant to 35 U.S.C. § 271.

27 28. AOS's acts of infringement have caused damage to Fairchild, and Fairchild is entitled
28 to recover from AOS the damages sustained as a result of AOS's wrongful acts in an amount subject to

1 proof at trial. AOS's infringement of Fairchild's exclusive rights under the '497 patent will continue to
2 cause damage to Fairchild, causing irreparable harm for which there is no adequate remedy at law
3 unless enjoined by this Court.

4 29. Upon information and belief, AOS's infringement of the '497 patent is willful and
5 deliberate, entitling Fairchild to increased damages under 35 U.S.C. § 284 and to attorneys' fees and
6 costs incurred in prosecuting this action under 35 U.S.C. § 285.

7 **SIXTH COUNTERCLAIM**
8 **(Infringement of U.S. Patent No. 6,828,195)**

9 30. Fairchild incorporates by reference and realleges paragraphs 1 through 5.

10 31. On December 7, 2004, United States Patent No. 6,828,195 ("the '195 patent"), entitled
11 "Method of Manufacturing a Trench Transistor Having a Heavy Body Region," was duly and legally
12 issued by the United States Patent and Trademark Office. Fairchild is the assignee of the '195 patent
13 and continues to hold all rights and interest in the '195 patent. A true and correct copy of the '195
14 patent is attached hereto as Exhibit D.

15 32. AOS has directly, indirectly, contributorily, and/or by inducement infringed and
16 continues to infringe the '195 patent by its manufacture, use, sale, importation, and/or offer for sale of
17 certain products, including without limitation, AOS power transistors. AOS is liable for its
18 infringement of the '195 patent pursuant to 35 U.S.C. § 271.

19 33. AOS's acts of infringement have caused damage to Fairchild, and Fairchild is entitled
20 to recover from AOS the damages sustained as a result of AOS's wrongful acts in an amount subject to
21 proof at trial. AOS's infringement of Fairchild's exclusive rights under the '195 patent will continue to
22 cause damage to Fairchild, causing irreparable harm for which there is no adequate remedy at law
23 unless enjoined by this Court.

24 34. Upon information and belief, AOS's infringement of the '195 patent is willful and
25 deliberate, entitling Fairchild to increased damages under 35 U.S.C. § 284 and to attorneys' fees and
26 costs incurred in prosecuting this action under 35 U.S.C. § 285.

SEVENTH COUNTERCLAIM
(Infringement of U.S. Patent No. 7,148,111)

35. Fairchild incorporates by reference and realleges paragraphs 1 through 5.

36. On December 12, 2006, United States Patent No. 7,148,111 ("the '111 patent"), entitled "Method of Manufacturing a Trench Transistor Having a Heavy Body Region," was duly and legally issued by the United States Patent and Trademark Office. Fairchild is the assignee of the '111 patent and continues to hold all rights and interest in the '111 patent. A true and correct copy of the '111 patent is attached hereto as Exhibit E.

37. AOS has directly, indirectly, contributorily, and/or by inducement infringed and continues to infringe the '111 patent by its manufacture, use, sale, importation, and/or offer for sale of certain products, including without limitation, AOS power transistors. AOS is liable for its infringement of the '111 patent pursuant to 35 U.S.C. § 271.

38. AOS's acts of infringement have caused damage to Fairchild, and Fairchild is entitled to recover from AOS the damages sustained as a result of AOS's wrongful acts in an amount subject to proof at trial. AOS's infringement of Fairchild's exclusive rights under the '111 patent will continue to cause damage to Fairchild, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

39. Upon information and belief, AOS's infringement of the '111 patent is willful and deliberate, entitling Fairchild to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

EIGHTH COUNTERCLAIM
(Infringement of U.S. Patent No. 6,818,947)

40. Fairchild incorporates by reference and realleges paragraphs 1 through 5.

41. On November 16, 2004, United States Patent No. 6,818,947 ("the '947 patent"), entitled "Buried State-Field Termination Structure," was duly and legally issued by the United States Patent and Trademark Office. Fairchild is the assignee of the '947 patent and continues to hold all rights and interest in the '947 patent. A true and correct copy of the '947 patent is attached hereto as Exhibit F.

42. AOS has directly, indirectly, contributorily, and/or by inducement infringed and continues to infringe the '947 patent by its manufacture, use, sale, importation, and/or offer for sale of certain products, including without limitation, AOS power transistors. AOS is liable for its infringement of the '947 patent pursuant to 35 U.S.C. § 271.

43. AOS's acts of infringement have caused damage to Fairchild, and Fairchild is entitled to recover from AOS the damages sustained as a result of AOS's wrongful acts in an amount subject to proof at trial. AOS's infringement of Fairchild's exclusive rights under the '947 patent will continue to cause damage to Fairchild, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

44. Upon information and belief, AOS's infringement of the '947 patent is willful and deliberate, entitling Fairchild to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

PRAAYER FOR RELIEF

WHEREFORE, Fairchild requests entry of judgment in its favor and against AOS as follows:

A. That the claims of AOS alleged in its Complaint be denied in their entirety and that AOS take nothing by way of its Complaint;

B. A declaration that Fairchild has not willfully or otherwise infringed, contributed to the infringement of, or actively induced others to infringe, and does not willfully or otherwise infringe, contribute to the infringement of, or actively induce others to infringe, any valid claim of the '776 and '567 patents;

C. A declaration that the claims of the '776 and '567 patents are invalid;

D. A judgment that AOS has infringed, and is infringing, the '481, '406, '497, '195, '111, and '947 patents;

E. A permanent injunction enjoining AOS and its respective officers, agents, employees, subsidiaries, and those acting in privity or concert with AOS, including related individuals and entities, customers, representatives, dealers, and distributors, from further infringement, contributory infringement and/or inducement of infringement of the '481, '406, '497, '195, '111, and '947 patents;

1 F. An award of damages arising out of AOS's infringement of the '481, '406, '497, '195,
2 '111, and '947 patents, including enhanced damages pursuant to 35 U.S.C. §284, together with
3 prejudgment and post-judgment interest, in an amount according to proof;

4 G. A declaration that this case is an exceptional case within the meaning of 35 U.S.C.
5 § 285 and an award of reasonable attorneys' fees to Fairchild; and

6 H. Costs of suit and such other and further relief as the Court deems just and proper.

7
8 DATED: September 28, 2007

Respectfully submitted,

9
10 By: /s/Eric P. Jacobs

Eric P. Jacobs

Peter H. Goldsmith

Robert A. McFarlane

Igor Shoiket

TOWNSEND AND TOWNSEND AND CREW LLP

Two Embarcadero Center, 8th Floor

San Francisco, California 94111

Telephone: (415) 576-0200

Facsimile: (415) 576-0300

11
12
13
14
15 Attorneys for Defendant

16 FAIRCHILD SEMICONDUCTOR CORPORATION
17
18
19
20
21
22
23
24
25
26
27
28

JURY DEMAND

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Fairchild demands a trial by jury on all issues so triable.

DATED: September 28, 2007

Respectfully submitted,

By: /s/Eric P. Jacobs

Eric P. Jacobs

Peter H. Goldsmith

Robert A. McFarlane

Igor Shoiket

TOWNSEND AND TOWNSEND AND CREW LLP

Two Embarcadero Center, 8th Floor

San Francisco, California 94111

Telephone: (415) 576-0200

Facsimile: (415) 576-0300

Attorneys for Defendant

FAIRCHILD SEMICONDUCTOR CORPORATION

61158933 v1

EXHIBIT A

US006429481B1

(12) **United States Patent**
Mo et al.

(10) **Patent No.:** **US 6,429,481 B1**
(45) **Date of Patent:** ***Aug. 6, 2002**

(54) **FIELD EFFECT TRANSISTOR AND
METHOD OF ITS MANUFACTURE**

(75) Inventors: **Brian Sze-Ki Mo**, Fremont; **Duc Chau**,
San Jose; **Steven Sapp**, Felton; **Izak**
Bencuya, Saratoga, all of CA (US);
Dean Edward Probst, West Jordan, UT
(US)

(73) Assignee: **Fairchild Semiconductor Corporation**,
South Portland, MA (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

4,345,265 A	8/1982	Blanchard	357/23
4,398,339 A	8/1983	Blanchard et al.	29/571
4,503,449 A	3/1985	David et al.	357/23.4
4,503,598 A	3/1985	Vora et al.	29/571
4,541,001 A	9/1985	Schutten et al.	357/23.4
4,639,762 A	1/1987	Neilson et al.	357/23.8

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP	0238749	9/1987
EP	0550770	7/1993
EP	0583028 A1	2/1994

(List continued on next page.)

OTHER PUBLICATIONS

S. M. Sze: "P-N-Junction Diode" *Physics of Semiconductor Devices Second Edition Bell Laboratories*, pp. 63-108 (1981).

(List continued on next page.)

(21) Appl. No.: **08/970,221**

(22) Filed: **Nov. 14, 1997**

(51) **Int. Cl.**⁷ **H01L 29/78**

(52) **U.S. Cl.** **257/341; 257/331**

(58) **Field of Search** **257/330, 245,**
257/497, 618, 341, 331

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,070,690 A	1/1978	Wickstrom	357/68
4,132,998 A	1/1979	Dingwall	357/23
4,145,703 A	3/1979	Blanchard et al.	357/55
4,326,332 A	4/1982	Kenney	
4,329,705 A	5/1982	Baker	357/43
4,344,081 A	8/1982	Pao et al.	357/43

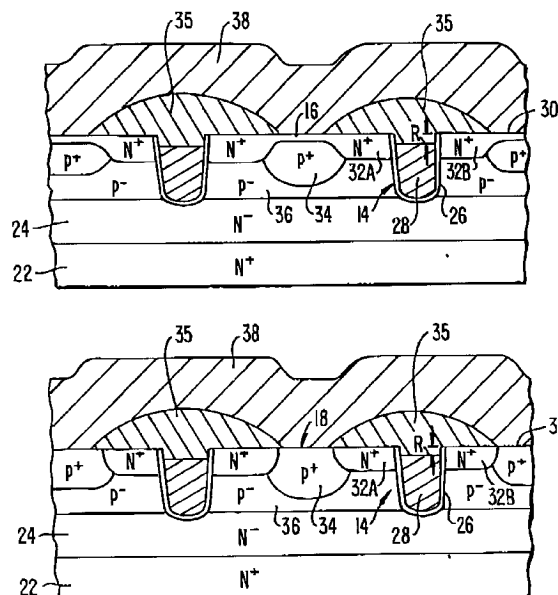
Primary Examiner—Jerome Jackson, Jr.

(74) *Attorney, Agent, or Firm*—Townsend and Townsend and Crew LLP

(57) **ABSTRACT**

A trench field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

22 Claims, 9 Drawing Sheets



US 6,429,481 B1

Page 2

U.S. PATENT DOCUMENTS

4,682,405 A	7/1987	Blanchard et al.	29/571	EP	0720236	3/1996	
4,683,643 A	8/1987	Nakajima et al.	437/203	EP	0746030	4/1996	
4,767,722 A	8/1988	Blanchard	437/41	EP	0 720 236	7/1996 H01L/29/78
4,808,543 A	2/1989	Parrillo et al.	437/38	EP	0 746 030	12/1996 H01L/27/02
4,845,537 A	7/1989	Nishimura et al.		EP	0 755 076	1/1997 H01L/29/739
4,860,072 A	8/1989	Zommer	357/23.8	EP	0755076	1/1997	
4,881,105 A	11/1989	Davari et al.		EP	0 795 911	9/1997 H01L/29/739
4,893,160 A	1/1990	Blanchard	357/23.4	EP	0795911	9/1997	
4,914,058 A	4/1990	Blanchard	437/203	EP	0801425	10/1997	
4,967,245 A	10/1990	Cogan et al.	357/23.4	EP	0 801 425	10/1997 H01L/29/10
4,983,535 A	1/1991	Blanchard	437/40	GB	2 269 050	1/1994 H01L/29/06
5,016,068 A	5/1991	Mori	357/23.5	GB	2269050 A	1/1994	
5,017,504 A	5/1991	Nishimura et al.		GB	2 269 050 A	1/1994	
5,045,900 A	9/1991	Tamagawa	357/23.4	JP	56131960	10/1981	
5,072,266 A	12/1991	Bulucea et al.		JP	57018365	1/1982	
5,124,764 A	6/1992	Mori	357/23.4	JP	57153469	9/1982	
5,160,491 A	11/1992	Mori	437/40	JP	58137254	8/1983	
5,168,331 A	12/1992	Yilmaz	257/331	JP	58210678	12/1983	
5,298,442 A	3/1994	Bulucea et al.	437/40	JP	59080970	5/1984	
5,298,780 A	3/1994	Harada		JP	59193064	11/1984	
5,316,959 A	5/1994	Kwan et al.	437/40	JP	60028271	2/1985	
5,341,011 A	8/1994	Hshieh et al.	257/330	JP	61102782	5/1986	
5,405,794 A	4/1995	Kim		JP	62012167	1/1987	
5,410,170 A	4/1995	Bulucea et al.	257/332	JP	62016572	1/1987	
5,430,324 A	7/1995	Bencuya		JP	62023171	1/1987	
5,455,190 A	10/1995	Hsu	437/40	JP	62046569	2/1987	
5,468,982 A	11/1995	Hshieh et al.	257/331	JP	63114173	5/1988	
5,474,943 A	12/1995	Hshieh et al.	437/40	JP	40 5-226661	* 9/1993 257/330
5,508,534 A	4/1996	Nakamura et al.		JP	08204194	8/1996	
5,532,179 A	7/1996	Chang et al.	437/40	JP	08250731	9/1996	
5,541,425 A	7/1996	Nishihara		JP	08316479	11/1996	
5,558,313 A	9/1996	Hshieh et al.	257/342	JP	09036362	2/1997	
5,567,634 A	10/1996	Hébert et al.		JP	09102607	4/1997	
5,578,851 A	11/1996	Hshieh et al.	257/330	JP	09270512	10/1997	
5,592,005 A	1/1997	Floyd et al.	257/331	WO	9303502	2/1993	
5,597,765 A	1/1997	Yilmaz et al.	437/203	WO	9534094	12/1995	
5,602,046 A	2/1997	Calafut et al.	437/41	WO	9707547	2/1997	
5,605,852 A	2/1997	Bencuya	437/40	WO	WO 97/16853	5/1997 H01L/29/10
5,614,751 A	3/1997	Yilmaz et al.	257/394				
5,629,543 A	5/1997	Hshieh et al.					
5,639,676 A	6/1997	Hsieh et al.	437/40 DM				
5,648,670 A	7/1997	Blanchard	257/329				
5,661,322 A	8/1997	Williams et al.					
5,665,619 A	9/1997	Kwan et al.					
5,665,996 A	9/1997	Williams et al.					
5,674,766 A	10/1997	Darwish et al.	437/40				
5,688,725 A	11/1997	Darwish et al.	438/270				
5,689,128 A	11/1997	Hshieh et al.	257/331				
5,701,026 A	12/1997	Fushima et al.	257/510				
5,767,550 A	6/1998	Calafut et al.	257/355				
5,783,491 A	7/1998	Nakamura et al.	438/702				
5,801,408 A	9/1998	Takahashi	257/212				
5,814,858 A	9/1998	Williams	257/328				
5,895,952 A	4/1999	Darwish et al.	257/330				
5,998,836 A	12/1999	Williams					
5,998,837 A	12/1999	Williams					
6,049,108 A	4/2000	Williams et al.					
6,204,533 B1	3/2001	Williams et al.					

FOREIGN PATENT DOCUMENTS

EP	0 698 919	2/1996 H01L/21/336
EP	0698919	2/1996	
EP	0720235	3/1996	

OTHER PUBLICATIONS

Homes, F. E.; Salama, C. A. T., "V Groove M.O.S. Transistor Technology," Electronic letters vol. 9, No. 19 (Sep. 20, 1973).

Homes, F. E.; Salama, C. A. T., "VMOS—A New MOS Integrated Circuit Technology," Solid-State Electronics, vol. 17, pp. 791–797 (1974).

Ou–Yang, Paul, "Double Ion Implanted V–MOS Technology," IEEE Journal of Solid–State Circuits, vol. SC–12, No. 1, pp. 3–10 (Feb. 1977).

Salama, C. Andre; Oakes, James G., "Nonplanar Power Field–Effect Transistor," IEEE Transactions on Electron Devices, vol. ED–25, No. 10, pp. 1222–1228 (Oct. 1978).

Lisiak, Kenneth P.; Berger, Josef, "Optimization of Nonplanar Power MOS Transistors," IEEE Transactions on Electron Devices, vol. ED–25, No. 10, pp. 1229–1234 (Oct. 1978).

Chang, T.S., et al, "Vertical FET Random–Access Memories with Deep Trench Isolation," IBM Technical Disclosure Bulletin, pp. 3683–3687 (Jan. 1980).

Sun, S. C., "Physics and Technology of Power MOSFETs," Stanford Electronics Laboratory, Integrated Circuits Laboratory, Technical Report No. IDEZ696–1 (Feb. 1982).

US 6,429,481 B1

Page 3

Blanchard, Richard A., "Optimization of Discrete High Power MOS Transistors," Stanford Electronics Laboratory, Integrated Circuits Laboratory, Technical Report No. IDEZ696-2 (Apr. 1982).

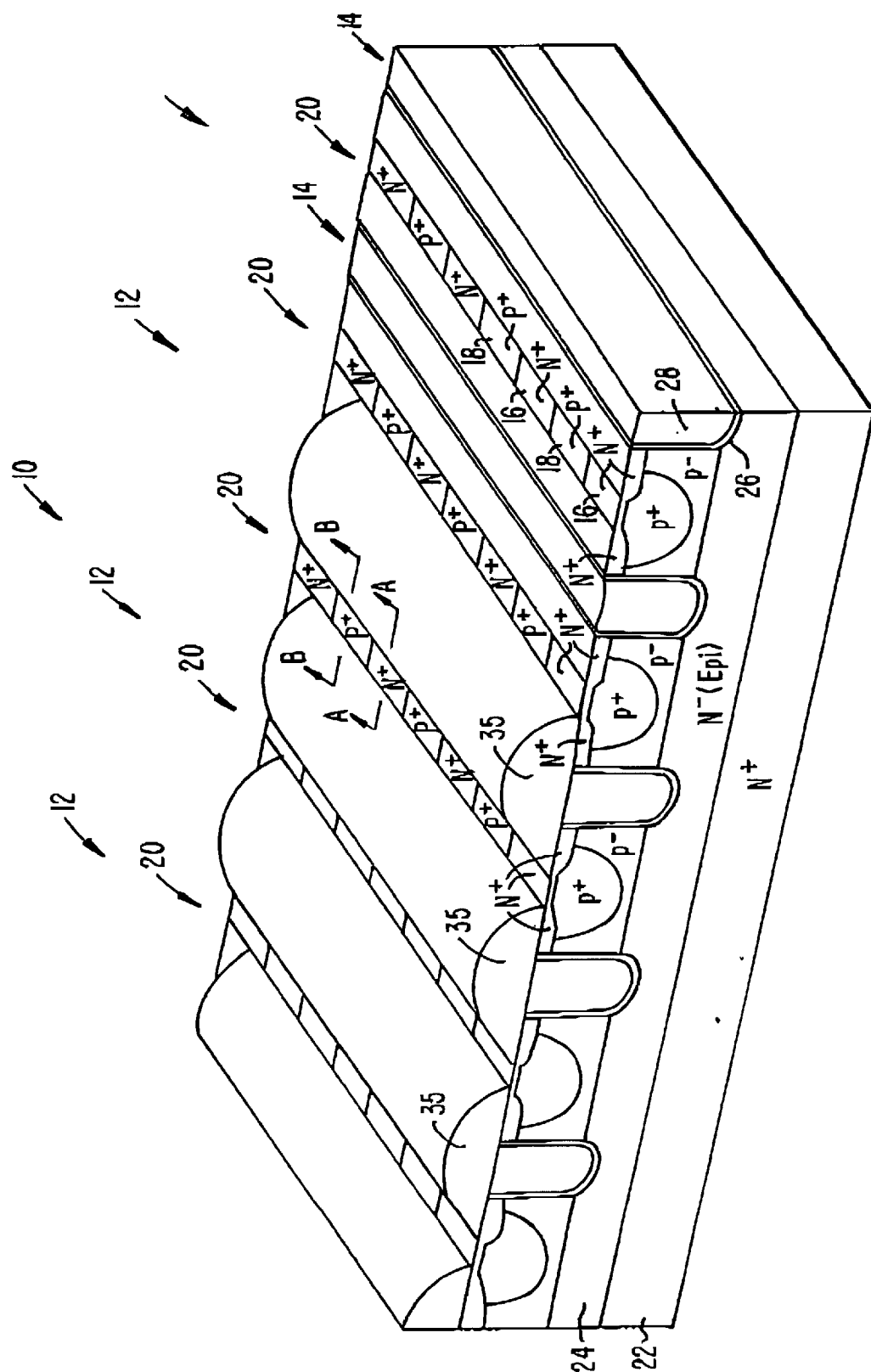
Frank Goodenough, Dense MOSFET Enables Portable Power Control, "Tech Insights", *Electronic Design*, Apr. 14, 1997.

Grant, D.A., Gowar, J.; "Power Mosfets: Theory and Applications," A. Wiley-Interscience Publication © 1989, pp. 5-23. [ISBN 0-471-82867-X].

"Power Mosfet Technology," Lidow et al., (International Electron Devices meeting, Dec. 3-5, 1979, *IEAM Technical Digest*, pp. 79-83.

"Optimization of Nonplanar Power MOS Transistors," Lisiak et al., *IEEE Transactions of Electron Devices*, vol. ED-25, No. 10, Oct. 1975, pp. 1229-1234.

* cited by examiner



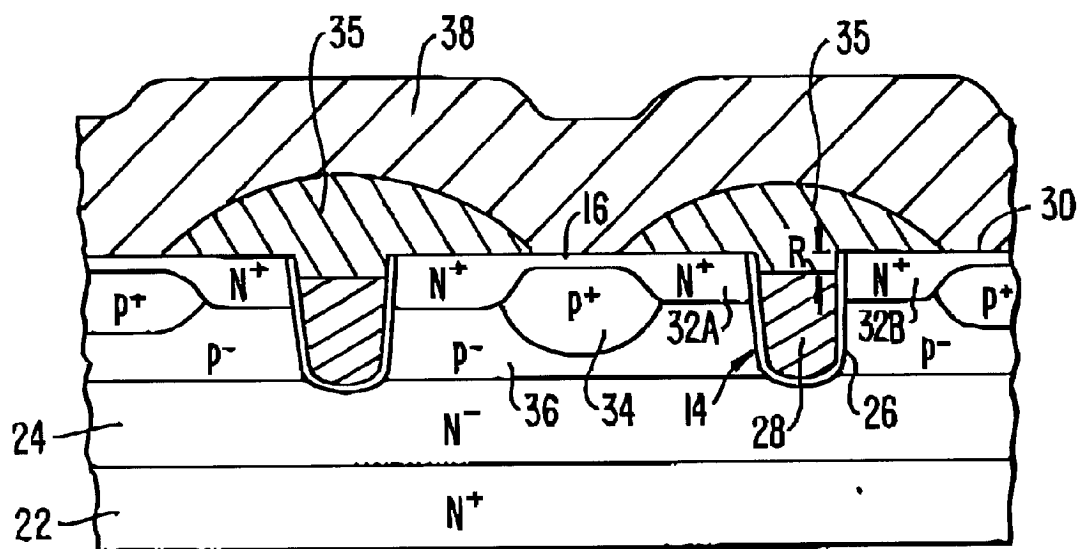


FIG. 1A.

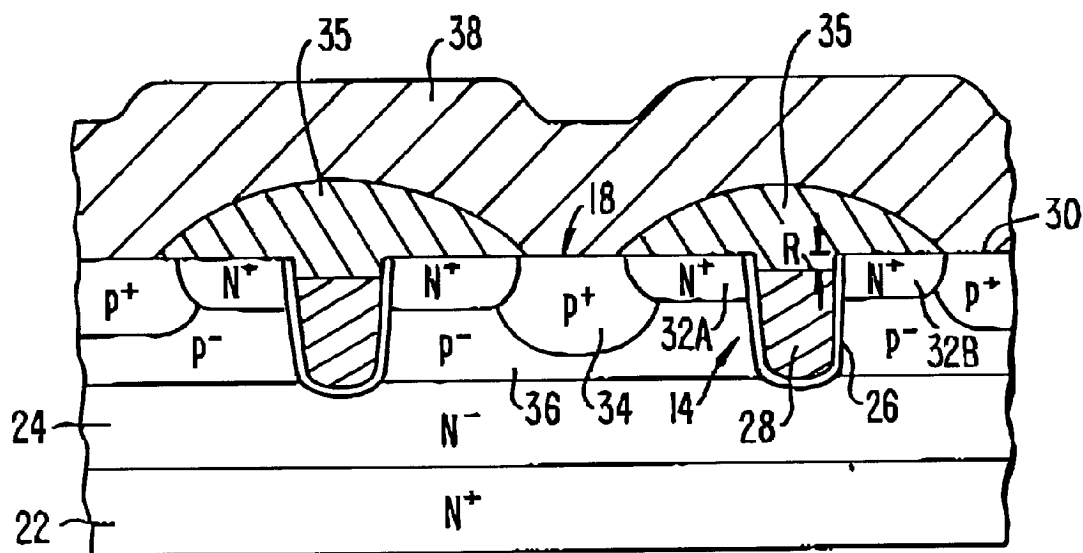


FIG. 1B.

U.S. Patent

Aug. 6, 2002

Sheet 3 of 9

US 6,429,481 B1

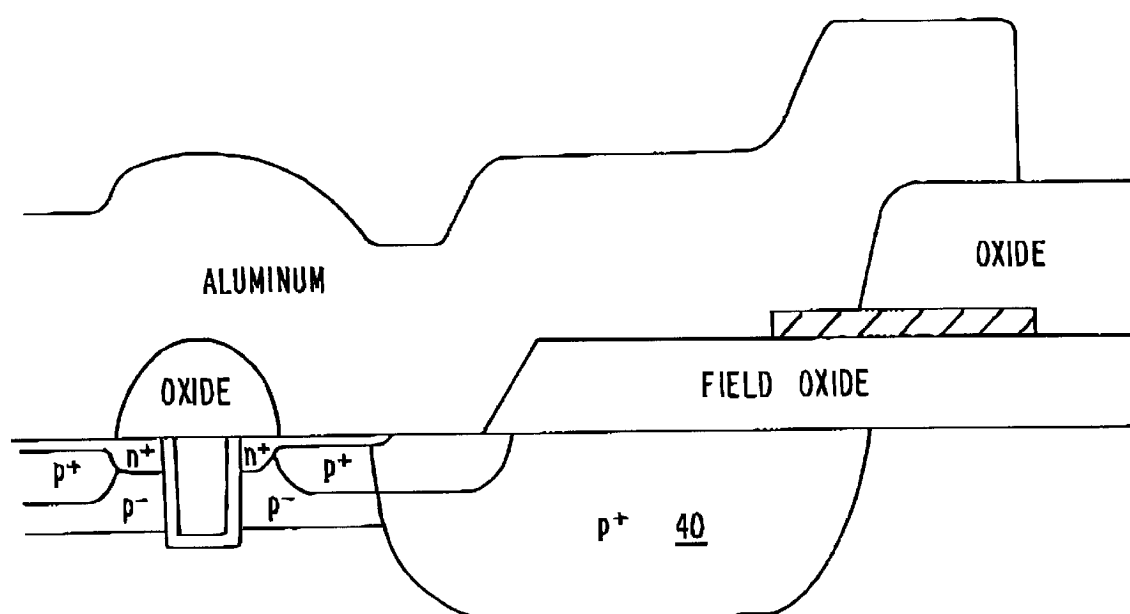


FIG. 2.

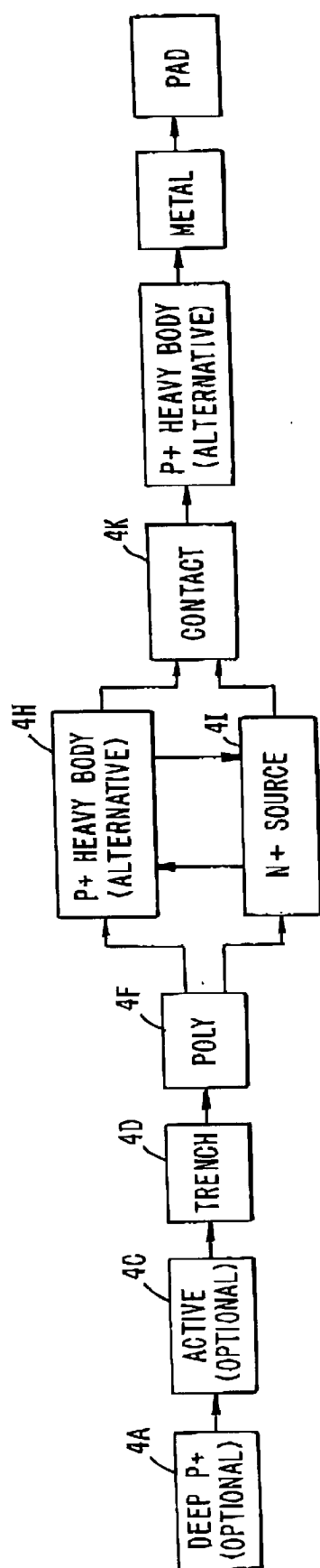


FIG. 3.

U.S. Patent

Aug. 6, 2002

Sheet 5 of 9

US 6,429,481 B1

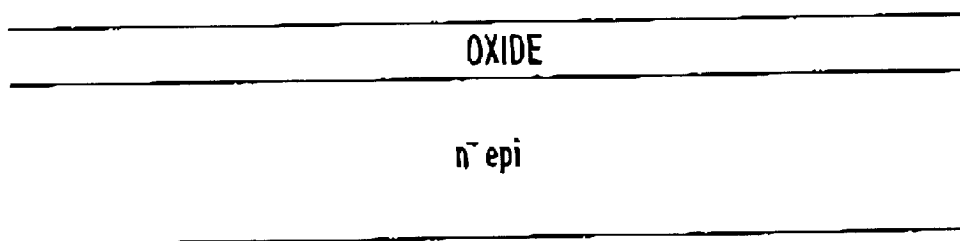


FIG. 4.

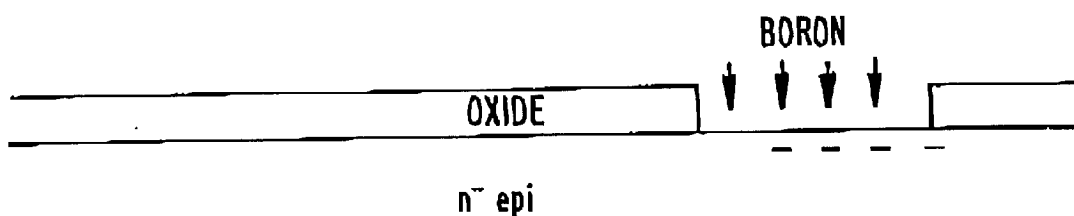


FIG. 4A.

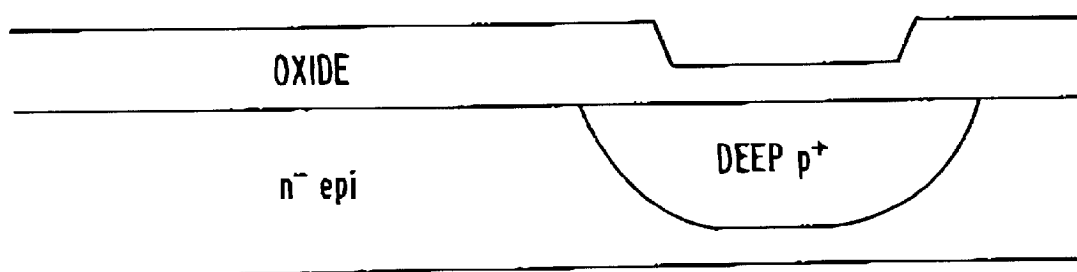


FIG. 4B.

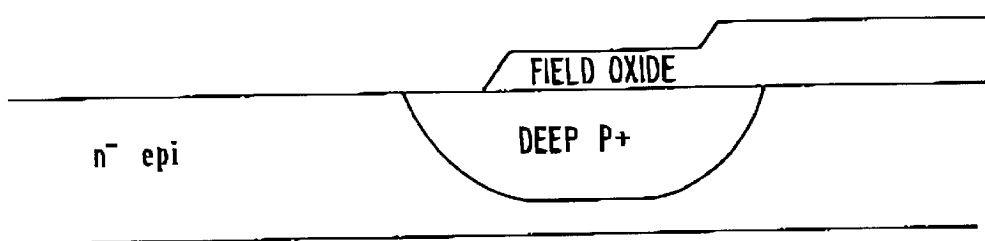


FIG. 4C.

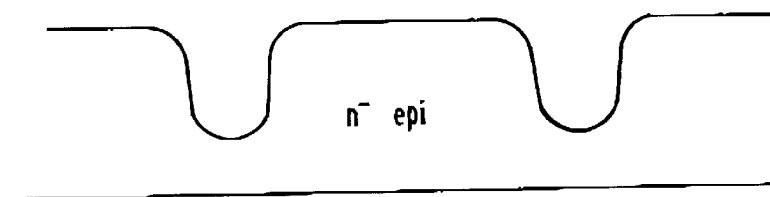


FIG. 4D.

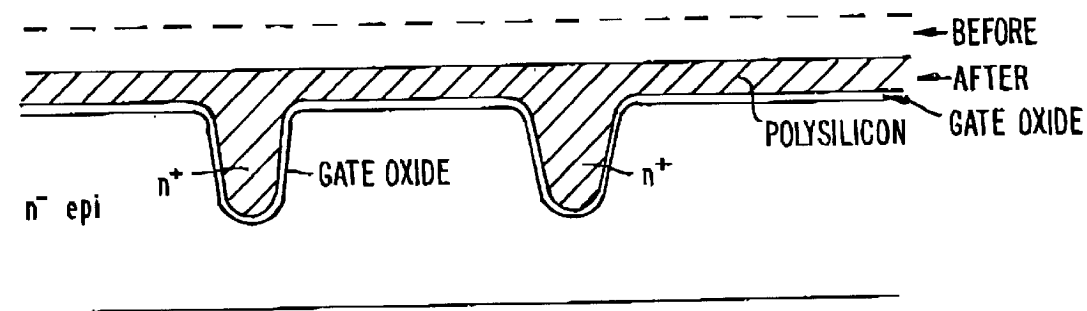


FIG. 4E.

U.S. Patent

Aug. 6, 2002

Sheet 7 of 9

US 6,429,481 B1

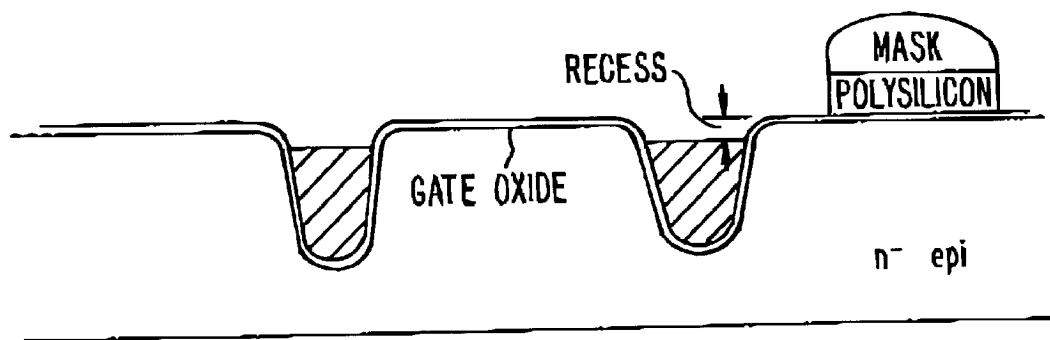


FIG. 4F.

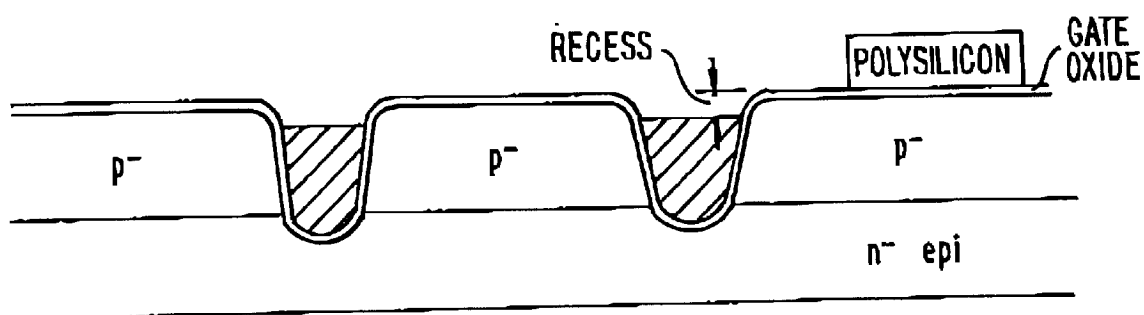


FIG. 4G.

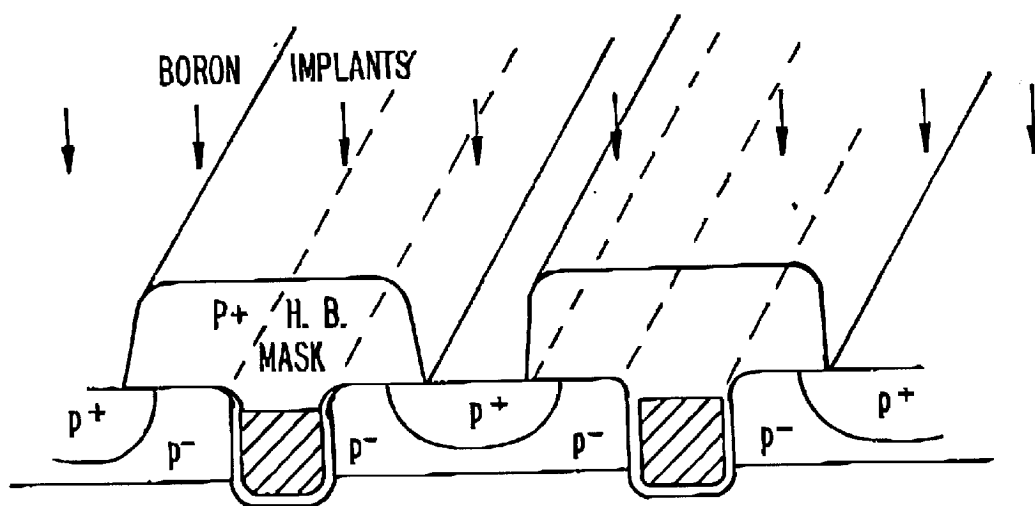


FIG. 4H.

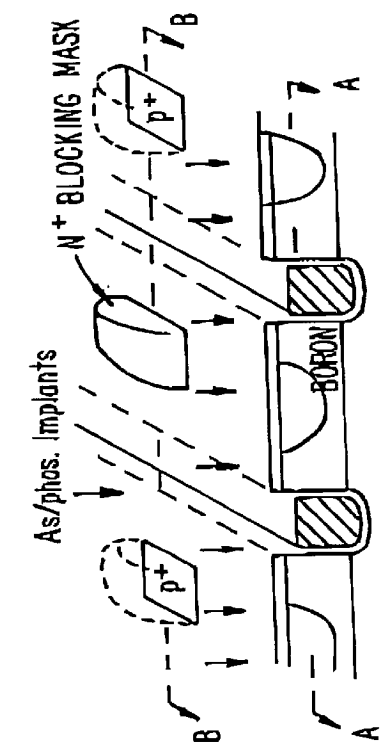


FIG. 4I.

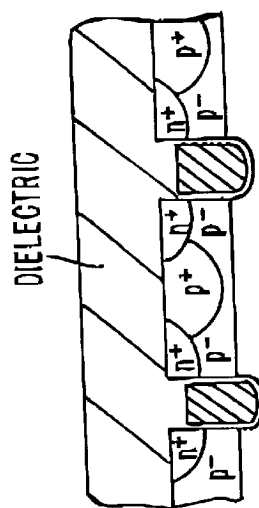
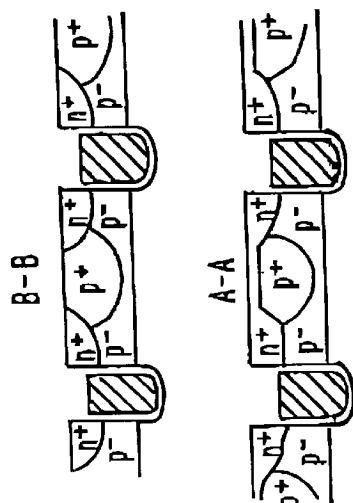


FIG. 4J.

BORON IMPLANTS (ALTERNATIVE)

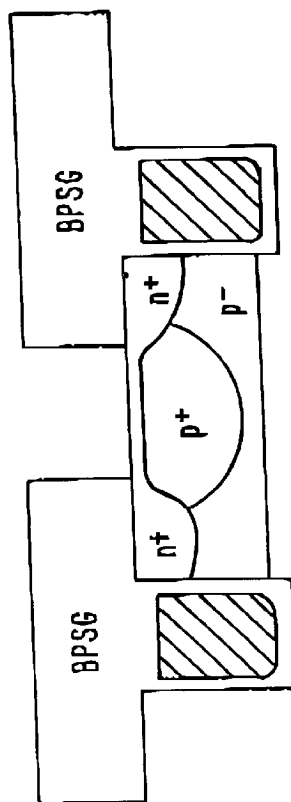


FIG. 4K.

U.S. Patent

Aug. 6, 2002

Sheet 9 of 9

US 6,429,481 B1

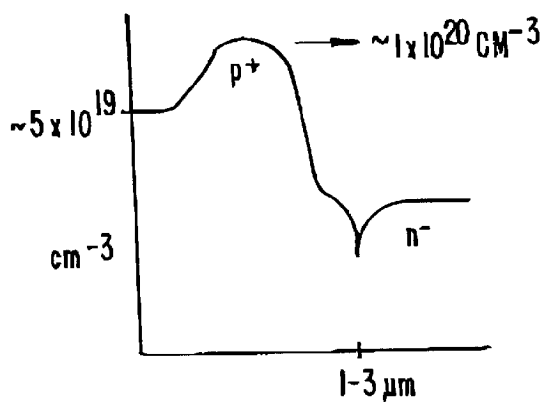


FIG. 5.

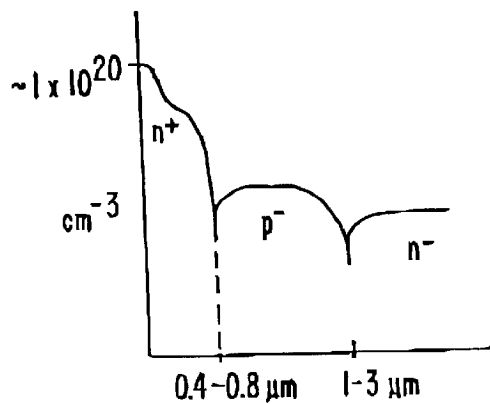


FIG. 5A.

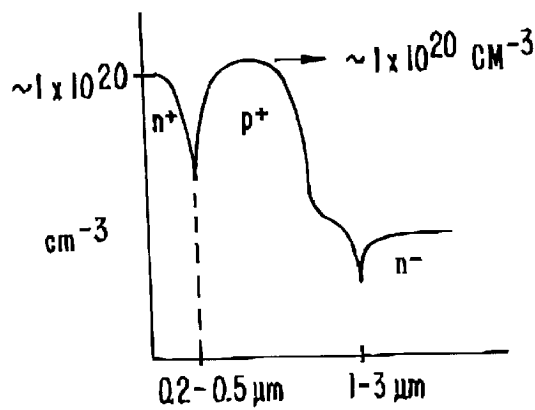


FIG. 5B.

US 6,429,481 B1

1

**FIELD EFFECT TRANSISTOR AND
METHOD OF ITS MANUFACTURE****BACKGROUND OF THE INVENTION**

The present invention relates to field effect transistors, in particular trench DMOS transistors, and methods of their manufacture.

Power field effect transistors, e.g., MOSFETs (metal oxide semiconductor field effect transistors), are well known in the semiconductor industry. One type of MOSFET is a DMOS (double diffused metal oxide semiconductor) transistor. DMOS transistors typically include a substrate on which an epitaxial layer is grown, a doped source junction, a doped heavy body, a doped well of the same (p or n) doping as the heavy body, and a gate electrode. In trench DMOS transistors the gate electrode is a vertical trench. The heavy body is typically diffused deeper than the bottom of the trench, to minimize electric field at the bottom corners of the trench and thereby prevent avalanche breakdown from damaging the device. The trench is filled with conductive polysilicon, and the polysilicon is generally overetched, to assure that it is completely removed from the surface surrounding the trench. This overetching generally leaves a recess between the top of the polysilicon and the surface of the semiconductor substrate (i.e., the surface of the epitaxial layer). The depth of this recess must be carefully controlled so that it is shallower than the depth of the source junctions. If the recess is deeper than the source junctions the source may miss the gate, resulting in high on-state resistance, high threshold, and potentially a non-functional transistor.

The source and drain junctions can be doped with either p-type or n-type dopants; in either case, the body will be doped with the opposite dopant, e.g., for n-type source and drain the body will be p-type. DMOS transistors in which the source and drain are doped with p-type carriers are referred to as "p-channel". In p-channel DMOS transistors a negative voltage applied to the transistor gate causes current flow from the source region, through a channel region of the body, an accumulation region of the epitaxial layer, and the substrate, to the drain region. Conversely, DMOS transistors, in which the source and drain are doped with n-type carriers, are referred to as "n-channel". In n-channel DMOS transistors a positive voltage applied to the transistor gate causes current to flow from drain to source.

It is desirable that DMOS transistors have low source to drain resistance ($R_{ds(on)}$) when turned on and low parasitic capacitance. The transistor structure should also avoid "punchthrough". Punchthrough occurs when, upon application of a high drain to source voltage, depletion into the body region extends to the source region, forming an undesirable conductive path through the body region when the transistor should be off. Finally, the transistor should have good "ruggedness", i.e., a high activation current is needed to turn on the parasitic transistor that inherently exists in DMOS transistors.

Generally a large number of MOSFET cells are connected in parallel forming a single transistor. The cells may be arranged in a "closed cell" configuration, in which the trenches are laid out in a grid pattern and the cells are enclosed on all sides by trench walls. Alternatively, the cells may be arranged in an "open cell" configuration, in which the trenches are laid out in a "stripe" pattern and the cells are only enclosed on two sides by trench walls. Electric field termination techniques are used to terminate junctions (doped regions) at the periphery (edges) of the silicon die on which the transistors are formed. This tends to cause the

2

breakdown voltage to be higher than it would otherwise be if controlled only by the features of the active transistor cells in the central portions of the die.

SUMMARY OF THE INVENTION

The present invention provides field effect transistors that have an open cell layout that provides good uniformity and high cell density and that is readily scalable. Preferred trench DMOS transistors exhibit low $R_{ds(on)}$, low parasitic capacitance, excellent reliability, resistance to avalanche breakdown degradation, and ruggedness. Preferred devices also include a field termination that enhances resistance to avalanche breakdown. The invention also features a method of making trench DMOS transistors.

In one aspect, the invention features a trench field effect transistor that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of the heavy body region relative to the depths of the well and the trench is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped well has a depth less than the predetermined depth of the trench. The trench has rounded top and bottom corners. There is an abrupt junction at the interface between the heavy body and the well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface.

In another aspect, the invention features an array of transistor cells. The array includes (a) a semiconductor substrate, (b) a plurality of gate-forming trenches arranged substantially parallel to each other and extending in a first direction, the space between adjacent trenches defining a contact area, each trench extending a predetermined depth into said substrate, the predetermined depth being substantially the same for all of said gate-forming trenches; (c) surrounding each trench, a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, (d) positioned between each pair of gate-forming trenches, a doped heavy body positioned adjacent each source junction, the deepest portion of each said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches, (e) a doped well surrounding each heavy body beneath the heavy body; and (f) p+ and n+ contacts disposed at the surface of the semiconductor substrate and arranged in alternation along the length of the contact area.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of each heavy body region relative to the depths of the wells and the gate-forming trenches is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped wells have a depth less than the predetermined depth of the trenches. The trenches have rounded top and bottom corners. There is an abrupt junction at the interface between each heavy body and the corresponding well, to cause the peak electric field, when voltage is applied to the transistor, to

US 6,429,481 B1

3

occur in the area of the interface. The array also includes a field termination structure surrounding the periphery of the array. The field termination structure includes a well having a depth greater than that of the gate-forming trenches. The field termination structure includes a termination trench extending continuously around the periphery of the array, more preferably a plurality of concentrically arranged termination trenches.

In yet another aspect, the invention features a semiconductor die that includes (a) a plurality of DMOS transistor cells arranged in an array on a semiconductor substrate, each DMOS transistor cell including a gate-forming trench, each of said gate-forming trenches having a predetermined depth, the depth of all of the gate-forming trenches being substantially the same; and (b) surrounding the periphery of the array, a field termination structure that extends into the semiconductor substrate to a depth that is deeper than said predetermined depth of said gate-forming trenches.

Preferred embodiments include one or more of the following features. The field termination structure includes a doped well. The field termination structure includes a termination trench. The field termination structure includes a plurality of concentrically arranged termination trenches. Each of the DMOS transistor cells further comprises a doped heavy body and the doped heavy body extends into the semiconductor substrate to a depth that is less than the predetermined depth of the gate-forming trenches.

The invention also features a method of making a heavy body structure for a trenched DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into said region a second dopant at a second energy and dosage, said second energy and dosage being relatively less than said first energy and dosage.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about 1E15 to 5E15. The second energy is from about 20 to 40 keV. The second dosage is from about 1E14 to 1E15.

Additionally, the invention features a method of making a source for a trenched DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into the region a second dopant at a second energy and dosage, the second energy and dosage being relatively less than the first energy and dosage.

Preferred embodiments include one or more of the following features. The first dopant comprises arsenic and the second dopant comprises phosphorus. The first energy is from about 80 to 120 keV. The first dosage is from about 5E15 to 1E16. The second energy is from about 40 to 70 keV. The second dosage is from about 1E15 to 5E15. The resulting depth of the source is from about 0.4 to 0.8 μm in the finished DMOS transistor.

In another aspect, the invention features a method of manufacturing a trenched field effect transistor. The method includes (a) forming a field termination junction around the perimeter of a semiconductor substrate, (b) forming an epitaxial layer on the semiconductor substrate, (c) patterning and etching a plurality of trenches into the epitaxial layer; (d) depositing polysilicon to fill the trenches, (e) doping the polysilicon with a dopant of a first type, (f) patterning the substrate and implanting a dopant of a second, opposite type

4

to form a plurality of wells interposed between adjacent trenches, (g) patterning the substrate and implanting a dopant of the second type to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned above the wells, each heavy body having an abrupt junction with the corresponding well, (h) patterning the substrate and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and (i) applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas.

Other features and advantages of the invention will be apparent from the following detailed description, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a highly enlarged, schematic perspective cross-sectional view showing a portion of a cell array including a plurality of DMOS transistors according to one aspect of the invention. The source metal layer and a portion of the dielectric layer have been omitted to show the underlying layers. FIGS. 1a and 1b are side cross-sectional views of a single line of transistors from the array of FIG. 1, taken along lines A—A and B—B, respectively. In FIGS. 1a and 1b the source metal and dielectric layers are shown.

FIG. 2 is a highly enlarged schematic side cross-sectional view of a semiconductor die showing a portion of the cell array and the field termination.

FIG. 3 is a flow diagram showing the photo mask sequence of a preferred process for forming a trench DMOS transistor of FIG. 1.

FIGS. 4-4k are schematic side cross-sectional views showing the individual steps of the process diagrammed in FIG. 3. The figure numbers for the detailed views in FIGS. 4-4k are shown parenthetically under the corresponding diagram boxes in FIG. 3.

FIGS. 5 and 5b are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A cell array 10, including a plurality of rows 12 of trenched DMOS transistors, is shown in FIG. 1. Cell array 10 has an open cell configuration, i.e., trenches 14 run in only one direction, rather than forming a grid. Individual cells are formed by alternating n+ source contacts 16 and p+ contacts 18 in rows 20 that run parallel to and between trenches 14. The configuration of the regions of each row that have an n+ source contact are shown in cross-section in FIG. 1a, while the regions that have a p+ contact are shown in FIG. 1b.

As shown in FIGS. 1a and 1b, each trenched DMOS transistor includes a doped n+ substrate (drain) layer 22, a more lightly doped n- epitaxial layer 24, and a gate electrode 28. Gate electrode 28 comprises a conductive polysilicon that fills a trench 14. A gate oxide 26 coats the walls of the trench and underlies the polysilicon. The top surface of the polysilicon is recessed from the surface 30 of the semiconductor substrate by a distance R (typically from about 0 to 0.4 μm). N+ doped source regions 32a, 32b are positioned one on each side of the trench 14. A dielectric layer 35 covers the trench opening and the two source regions 32a, 32b. Extending between the source regions of adjacent cells is a p+ heavy body region 34 and, beneath it,

US 6,429,481 B1

5

a flat-bottomed p- well **36**. In the areas of the cell array which have a n+ contact **16**, a shallow n+ doped contact region extends between the n+ source regions. A source metal layer **38** covers the surface of the cell array.

The transistor shown in FIGS. **1a** and **1b** includes several features that enhance the ruggedness of the transistor and its resistance to avalanche breakdown degradation.

First, the depth of the p+ heavy body region **34** relative to the depths of the trench **14** and the flat bottom of the p- well is selected so that the peak electric field when voltage is applied to the transistor will be approximately halfway between adjacent trenches. The preferred relative depths of the p+ heavy body, the p- well and the trench are different for different device layouts. However, preferred relative depths can be readily determined empirically (by observing the location of peak electric field) or by finite element analysis.

Second, the bottom corners of the trench **14** are rounded (preferably, the top corners are also rounded; this feature is not shown). Corner rounding can be achieved using the process described in copending application U.S. Ser. No. 08/959,197, filed on Oct. 28, 1997. The rounded corners of the trench also tend to cause the peak electric field to be moved away from the trench corners and towards a central location between adjacent trenches.

Third, an abrupt junction at the interface between the p+ heavy body and the p- well causes the peak electric field to occur in that area of the interface. Avalanche multiplication initiates at the location of the peak electric field, thus steering hot carriers away from the sensitive gate oxide and channel regions. As a result, this structure improves reliability and avalanche ruggedness without sacrificing cell density as much as a deeper heavy body junction. This abrupt junction can be achieved by the double doping process that will be described below, or by other processes for forming abrupt junctions, many of which are known in the semiconductor field.

Lastly, referring to FIG. **2**, the cell array is surrounded by a field termination junction **40** which increases the breakdown voltage of the device and draws avalanche current away from the cell array to the periphery of the die. Field termination junction **40** is a deep p+ well, preferably from about 1 to 3 μm deep at its deepest point, that is deeper than the p+ heavy body regions **34** in order to reduce the electric field caused by the junction curvature. A preferred process for making the above-described transistors is shown as a flow diagram in FIG. **3**, and the individual steps are shown schematically in FIGS. **4-4k**. It is noted that some steps that are conventional or do not require illustration are described below but not shown in FIGS. **4-4k**. As indicated by the arrows in FIG. **3**, and as will be discussed below, the order of the steps shown in FIGS. **4-4k** can be varied. Moreover, some of the steps shown in FIGS. **4-4k** are optional, as will be discussed.

A semiconductor substrate is initially provided. Preferably, the substrate is a N++ Si substrate, having a standard thickness, e.g., 500 μm , and a very low resistivity, e.g., 0.001 to 0.005 Ohm-cm. An epitaxial layer is deposited onto this substrate, as is well known, preferably to a thickness of from about 4 to 10 μm . Preferably the resistivity of the epitaxial layer is from about 0.1 to 3.0 Ohm-cm.

Next, the field termination junction **40** is formed by the steps shown in FIGS. **4-4c**. In FIG. **4**, an oxide layer is formed on the surface of the epitaxial layer. Preferably, the thickness of the oxide is from about 5 to 10 kÅ. Next, as shown in FIG. **4a**, the oxide layer is patterned and etched to

6

define a mask, and the p+ dopant is introduced to form the deep p+ well field termination. A suitable dopant is boron, implanted at an energy of from about 40 to 100 keV and a dose of $1\text{E}14$ (1×10^{14}) to $1\text{E}16$ cm^{-2} . As shown in FIG. **4b**, the p+ dopant is then driven further into the substrate, e.g., by diffusion, and a field oxide layer is formed over the p+ junction. Preferably the oxide thickness is from about 4 to 10 kÅ. Finally, the oxide (FIG. **4**) over the active area of the substrate (the area where the cell array will be formed) is patterned and removed by any suitable etching process, leaving only the field oxide in suitable areas. This leaves the substrate ready for the following steps that will form the cell array.

It is noted that, as an alternative to steps **4-4c**, a suitable field termination structure can be formed using a ring-shaped trench which surrounds the periphery of the cell array and acts to lessen the electric field and increase the resistance to avalanche breakdown degradation. This trench field termination does not require a field oxide or deep p+ body junction to be effective. Consequently, it can be used to reduce the number of process steps. Using a trench ring (or multiple concentric trench rings) to form a field termination is described in, e.g., U.S. Pat. No. 5,430,324, the full disclosure of which is hereby incorporated herein by reference. Preferably, the trench would have substantially the same depth as the trenches in the cell array.

The cell array is formed by the steps shown in FIGS. **4d-4k**. First, a plurality of trenches are patterned and etched into the epitaxial layer of the substrate (FIG. **4d**). Preferably, as noted above, the trenches are formed using the process described in copending application U.S. Ser. No. 08/959, 197, so that the upper and lower corners of each trench will be smoothly rounded. As shown in FIG. **1** and described above, the trenches are patterned to run in only one direction, defined as an open cell structure. After trench formation, a gate oxide layer is formed on the trench walls, as is well known in the semiconductor field. Preferably the gate oxide has a thickness of from about 100 to 800 Å.

Next, as shown in FIG. **4e**, polysilicon is deposited to fill the trench and cover the surface of the substrate, generally to a thickness of from about 1 to 2 μm depending on the trench width (shown by the dotted lines in FIG. **4e**). This layer is then planarized by the nature of its thickness relative to the trench width, typically from about 2 to 5 kÅ (indicated by solid lines in FIG. **4e**). The polysilicon is then doped to n-type, e.g., by conventional POCL_3 doping or by phosphorus implant. The backside of the wafer need not be stripped (as is conventionally done prior to doping the polysilicon to enhance defect gettering) because any further doping of the highly doped substrate would be unlikely to result in any enhancement in defect gettering.

The polysilicon is then patterned with a photoresist mask and etched to remove it from the trench areas, as shown in FIG. **4f**. A small recess between the top of the polysilicon in the trench and the substrate surface inherently results when the polysilicon is etched completely to remove all of the polysilicon from the substrate surface. The depth of this recess must be controlled so that it does not exceed the depth of the n+ source junction that will be formed in a later step. To reduce the need to carefully control this aspect of the process, a relatively deep n+ source junction is formed, as will be discussed below.

Then, as shown in FIG. **4g**, the p- well is formed by implanting the dopant, e.g., a boron implant at an energy of 30 to 100 keV and a dosage of $1\text{E}13$ to $1\text{E}15$, and driving it in to a depth of from about 1 to 3 μm using conventional drive in techniques.

US 6,429,481 B1

7

The next two steps (p+ heavy body formation) can be performed either before formation of the n+ source junction, or afterwards, as indicated by the arrows in FIG. 3. P+ heavy body formation and n+ source junction formation can be performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. 4h. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. 4k, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p- well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of 1E15 to 5E15, and a second boron implant at an energy of 20 to 40 keV and a dose of 1E14 to 1E15. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact 18. The resulting p+ heavy body junction is preferably about 0.4 to 1 μm deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5 μm deep), and includes a region of high dopant concentration near the interface with the p- well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. 5.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts 18 (FIGS. 1 and 1b), as shown in FIG. 4i. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. 4i, which correspond to FIGS. 1a and 1b).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of 5E15 to 1E16 followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of 1E15 to 5E15. The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8 μm after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts 16 (see FIGS. 1 and 1a) by compensating (converting) the p-type surface of the p+

8

heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. 5a and 5b, respectively.

Thus, the alternating p+ and n+ contacts 18, 16, shown in FIG. 1 are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower $R_{ds, on}$.

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900° C., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. 4j), after which the dielectric is patterned and etched (FIG. 4k) to define electrical contact openings over the n+ and p+ contacts 16, 18.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well known in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "n" doped instead, and vice versa.

What is claimed is:

1. A trenched field effect transistor comprising:

- a semiconductor substrate having dopants of a first conductivity type;
- a trench extending a predetermined depth into said semiconductor substrate;
- a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;
- a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and
- a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,

wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.

US 6,429,481 B1

9

2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.

3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.

4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.

5. The trenched field effect transistor of claim 4 wherein said doped heavy body has a first dopant concentration near the abrupt junction and a second dopant concentration near its upper surface that is less than the first dopant concentration.

6. An array of transistor cells comprising:

a semiconductor substrate having a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending a predetermined depth into said substrate and the space between adjacent trenches defining a contact area;

a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type;

a doped well having a second conductivity type with a charge opposite that of the first conductivity type, the doped well formed in the semiconductor substrate between each pair of gate-forming trenches;

a doped heavy body having the second conductivity type formed inside the doped well and positioned adjacent each source junction, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and

alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction with the well, and a depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.

7. The array of transistor cells of claim 6, wherein each said doped well has a substantially flat bottom.

8. The array of transistor cells of claim 6 wherein the controlled depth of the junction causes the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches.

9. The array of transistor cells of claim 6 wherein each said doped well has a depth less than the predetermined depth of said gate-forming trenches.

10. The array of transistor cells of claim 6 wherein each said gate-forming trench has rounded top and bottom corners.

11. The array of transistor cells of claim 9 further comprising a field termination structure surrounding the periphery of the array.

12. The array of transistor cells of claim 11 wherein said field termination structure comprises a well having a depth greater than that of the gate-forming trenches.

10

13. The array of transistor cells of claim 11 wherein said field termination structure comprises a termination trench extending continuously around the periphery of the array.

14. The array of transistor cells of claim 13 wherein said field termination structure comprises a plurality of concentrically arranged termination trenches.

15. A trenched field effect transistor formed on a substrate, comprising:

a plurality of trenches formed in parallel along a longitudinal axis, the plurality of trenches extending into the substrate to a first depth;

a doped well extending into the substrate between each pair of trenches;

a pair of doped source regions formed on opposite sides of each trench; and

a doped heavy body formed inside the doped well adjacent each source region, the doped heavy body extending into the doped well to a second depth that is less than the first depth,

wherein the doped heavy body:

forms a continuous doped region along substantially the entire longitudinal axis of a trench, and

forms an abrupt junction with the well, and a depth of the heavy body junction relative to a maximum depth of the well, is adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor.

16. The trenched field effect transistor of claim 15 further comprising source and heavy body contact areas defined on a surface of the substrate between each pair of trenches.

17. The trenched field effect transistor of claim 16 wherein the contact areas alternate between source and heavy body contacts.

18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.

19. The semiconductor die of claim 18 wherein said field termination structure comprises a deep doped well.

20. The trenched field effect transistor of claim 19 wherein said double implant comprises a first high energy implant to reach said second depth, and a second lower energy implant to extend the heavy body from said second depth to substantially a surface of the substrate.

21. The trenched field effect transistor of claim 6, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well, with no buried layer formed at an interface between the epitaxial layer and the substrate.

22. The trenched field effect transistor of claim 15, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well,

wherein the second depth relative to a depth of the well is adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,429,481 B1
DATED : August 6, 2002
INVENTOR(S) : Mo et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4,

Line 38, should read -- Figs. 5, 5a and 5b are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor. --

Signed and Sealed this

Twenty-fifth Day of May, 2004

A handwritten signature in black ink, reading "Jon W. Dudas". The signature is stylized, with a large loop for the "J" and a cursive "Dudas".

JON W. DUDAS
Acting Director of the United States Patent and Trademark Office

EXHIBIT B

(12) **United States Patent**
Mo et al.

(10) **Patent No.:** **US 6,710,406 B2**
(45) **Date of Patent:** ***Mar. 23, 2004**

(54) **FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE**

(75) Inventors: **Brian Sze-Ki Mo**, Fremont, CA (US); **Duc Chau**, San Jose, CA (US); **Steven Sapp**, Felton, CA (US); **Izak Bencuya**, Saratoga, CA (US); **Dean Edward Probst**, West Jordan, UT (US)

(73) Assignee: **Fairchild Semiconductor Corporation**, South Portland, ME (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 35 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/155,554**

(22) Filed: **May 24, 2002**

(65) **Prior Publication Data**

US 2002/0140027 A1 Oct. 3, 2002

Related U.S. Application Data

(63) Continuation of application No. 08/970,221, filed on Nov. 14, 1997, now Pat. No. 6,429,481.

(51) **Int. Cl.⁷** **H01L 29/78**
(52) **U.S. Cl.** **257/341; 257/331**
(58) **Field of Search** **257/331, 341**

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,070,690 A	1/1978	Wickstrom
4,132,998 A	1/1979	Dingwall
4,145,703 A	3/1979	Blanchard et al.
4,326,332 A	4/1982	Kenney
4,329,705 A	5/1982	Baker
4,344,081 A	8/1982	Pao et al.
4,345,265 A	8/1982	Blanchard

4,398,339 A	8/1983	Blanchard et al.
4,503,449 A	3/1985	David et al.
4,503,598 A	3/1985	Vora et al.
4,541,001 A	9/1985	Schutten et al.

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

CN	1090680 A	4/1994
EP	0 238 749 A2	9/1987
EP	0 550 770 B1	7/1993

(List continued on next page.)

OTHER PUBLICATIONS

Blanchard, R.A., "Optimization of discrete high power MOS transistors," *Stanford Electronics Laboratory, Integrated Circuits Laboratory*, Apr. 1982, Technical Report No. IDEZ696-2.

Chang, T.S. and Critchlow, D.L., "Verticle FET random-access memories with deep trench isolation," *IBM Technical Disclosure Bulletin*, Jan. 1980, pp. 3683-3687, vol. 22(8B).
Grant, D.A. and Gower, J., "The development of power MOS devices," Chapter 1.2 *In Power Mosfets: Theory and applications*. John Wiley & Sons; New York, 1989, pp. 5-23.

(List continued on next page.)

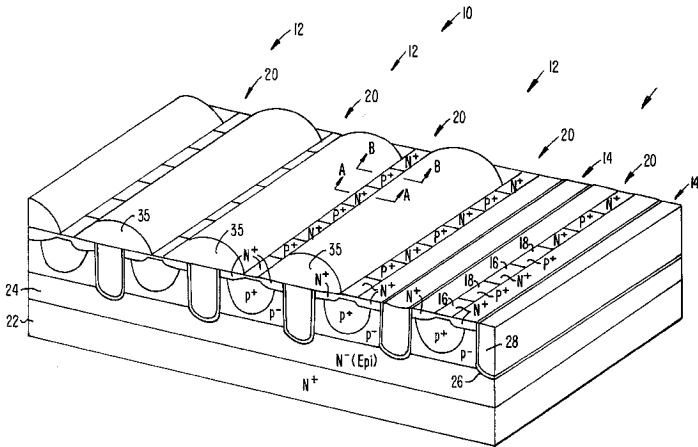
Primary Examiner—Jerome Jackson

(74) *Attorney, Agent, or Firm*—Babak S. Sani; Townsend and Townsend and Crew LLP

(57) **ABSTRACT**

A trench field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

32 Claims, 9 Drawing Sheets



US 6,710,406 B2

Page 2

U.S. PATENT DOCUMENTS

4,639,762 A 1/1987 Neilson et al.
 4,682,405 A 7/1987 Blanchard et al.
 4,683,643 A 8/1987 Nakajima et al.
 4,767,722 A 8/1988 Blanchard
 4,808,543 A 2/1989 Parrillo et al.
 4,845,537 A 7/1989 Nishimura et al.
 4,860,072 A 8/1989 Zommer
 4,881,105 A 11/1989 Davari et al.
 4,893,160 A 1/1990 Blanchard
 4,914,058 A 4/1990 Blanchard
 4,967,245 A 10/1990 Cogan et al.
 4,983,535 A 1/1991 Blanchard
 5,016,068 A 5/1991 Mori
 5,017,504 A 5/1991 Nishimura et al.
 5,045,900 A 9/1991 Tamagawa
 5,072,266 A 12/1991 Bulucea et al.
 5,124,764 A 6/1992 Mori
 5,160,491 A 11/1992 Mori
 5,168,331 A 12/1992 Yilmaz
 5,298,442 A 3/1994 Bulucea et al.
 5,298,780 A 3/1994 Harada
 5,316,959 A 5/1994 Kwan et al.
 5,321,289 A 6/1994 Baba et al.
 5,341,011 A 8/1994 Hshieh et al.
 5,405,794 A 4/1995 Kim
 5,410,170 A 4/1995 Bulucea et al.
 5,430,324 A 7/1995 Bencuya
 5,455,190 A 10/1995 Hsu
 5,460,985 A 10/1995 Tokura et al.
 5,468,982 A 11/1995 Hshieh et al.
 5,474,943 A 12/1995 Hshieh et al.
 5,508,534 A 4/1996 Nakamura et al.
 5,532,179 A 7/1996 Chang et al.
 5,541,425 A 7/1996 Nishihara
 5,558,313 A 9/1996 Hshieh et al.
 5,567,634 A 10/1996 Hébert et al.
 5,578,851 A 11/1996 Hshieh et al.
 5,592,005 A 1/1997 Floyd et al.
 5,597,765 A 1/1997 Yilmaz et al.
 5,602,046 A 2/1997 Calafut et al.
 5,605,852 A 2/1997 Bencuya
 5,614,751 A 3/1997 Yilmaz et al.
 5,629,543 A 5/1997 Hshieh et al.
 5,639,676 A 6/1997 Hshieh et al.
 5,648,670 A 7/1997 Blanchard
 5,661,322 A 8/1997 Williams et al.
 5,665,619 A 9/1997 Kwan et al.
 5,665,996 A 9/1997 Williams et al.
 5,674,766 A 10/1997 Darwish et al.
 5,688,725 A 11/1997 Darwish et al.
 5,689,128 A 11/1997 Hshieh et al.
 5,701,026 A 12/1997 Fujishima et al.
 5,767,550 A 6/1998 Calafut et al.
 5,776,812 A 7/1998 Takahashi et al.
 5,780,324 A 7/1998 Tokura et al.
 5,783,491 A 7/1998 Nakamura et al.
 5,783,915 A 7/1998 Shida et al.
 5,801,408 A 9/1998 Takahashi
 5,814,858 A 9/1998 Williams
 5,879,971 A 3/1999 Witek
 5,895,952 A 4/1999 Darwish et al.
 5,930,630 A 7/1999 Hshieh et al.
 5,986,304 A 11/1999 Hshieh et al.
 5,998,836 A 12/1999 Williams
 5,998,837 A 12/1999 Williams
 6,015,737 A 1/2000 Tokura et al.
 6,049,108 A 4/2000 Williams et al.
 6,204,533 B1 3/2001 Williams et al.

FOREIGN PATENT DOCUMENTS

EP 0 583 028 A1 2/1994
 EP 0 698 919 A2 2/1996
 EP 0 720 235 A2 7/1996
 EP 0 720 236 A2 7/1996
 EP 0 746 030 A3 12/1996
 EP 0 746 030 A2 12/1996
 EP 0 755 076 A2 1/1997
 EP 0 795 911 A2 9/1997
 EP 0 801 425 A1 10/1997
 GB 2269050 A 1/1994
 JP 56131960 A 10/1981
 JP 57018365 A 1/1982
 JP 57153469 A 9/1982
 JP 58137254 A 8/1983
 JP 58210678 A 12/1983
 JP 59080970 A 5/1984
 JP 59193064 A 11/1984
 JP 60028271 A 2/1985
 JP 61102782 A 5/1986
 JP 62012167 A 1/1987
 JP 62016572 A 1/1987
 JP 62023171 A 1/1987
 JP 62046569 A 2/1987
 JP 63114173 A 5/1988
 JP 05226661 A 9/1993
 JP 08204194 A 8/1996
 JP 08250731 A 9/1996
 JP 08316479 A 11/1996
 JP 09036362 A 2/1997
 JP 09102607 A 4/1997
 JP 09270512 A 10/1997
 WO 93/03502 A1 2/1993
 WO 95/34094 A1 12/1995
 WO 97/07547 A1 2/1997
 WO 97/16853 A1 5/1997

OTHER PUBLICATIONS

Goodenough, F., "Dense MOSFET enables portable power control," *Electronic Design* Apr. 14, 1997, pp. 45–50.

Holmes, F.E., and Salama, C.A.T., "V groove M.O.S. transistor technology," *Electronic Letters*, Sep. 20, 1973, pp. 457–458, vol. 9(19).

Holmes, F.E., and Salama, C.A.T., "VMOS—A new MOS integrated circuit technology," *Solid State Electronics* 1974, pp. 791–797, vol. 17.

Lidow, A. et al., "Power Mosfet technology," *IEEE Technical Digest—Int. Electron Devices Meet.* 1979, pp. 79–83.

Lisiak, K.P. and Berger, J., "Optimization of nonplanar power MOS transistors," *IEEE Transactions on Electron Devices*, Oct. 1978, pp. 1229–1234, vol. Ed–25(10).

Ou–Yang, P., "Double ion implanted V–MOS technology," *IEEE Journal of Solid–State Circuits*, Feb. 1977, pp. 3–10, vol. SC–12(1).

Salama, C.A. and Oakes, J.G., "Nonplanar power field–effect transistors," *IEEE Transactions on Electron Devices*, Oct. 1978, pp. 1222–1228, vol. Ed–25(10).

Sun, S.C., "Physics and technology of power MOSFETs," *Stanford Electronics Laboratory, Integrated Circuits Laboratory*, Feb. 1982, Technical Report No. IDEZ696–1.

Sze, S.M., "P–N– Junction diode," Chapter 2 *In Physics of Semiconductor Devices*. Second Edition, John Wiley & Sons; New York, 1981, pp. 63–108.

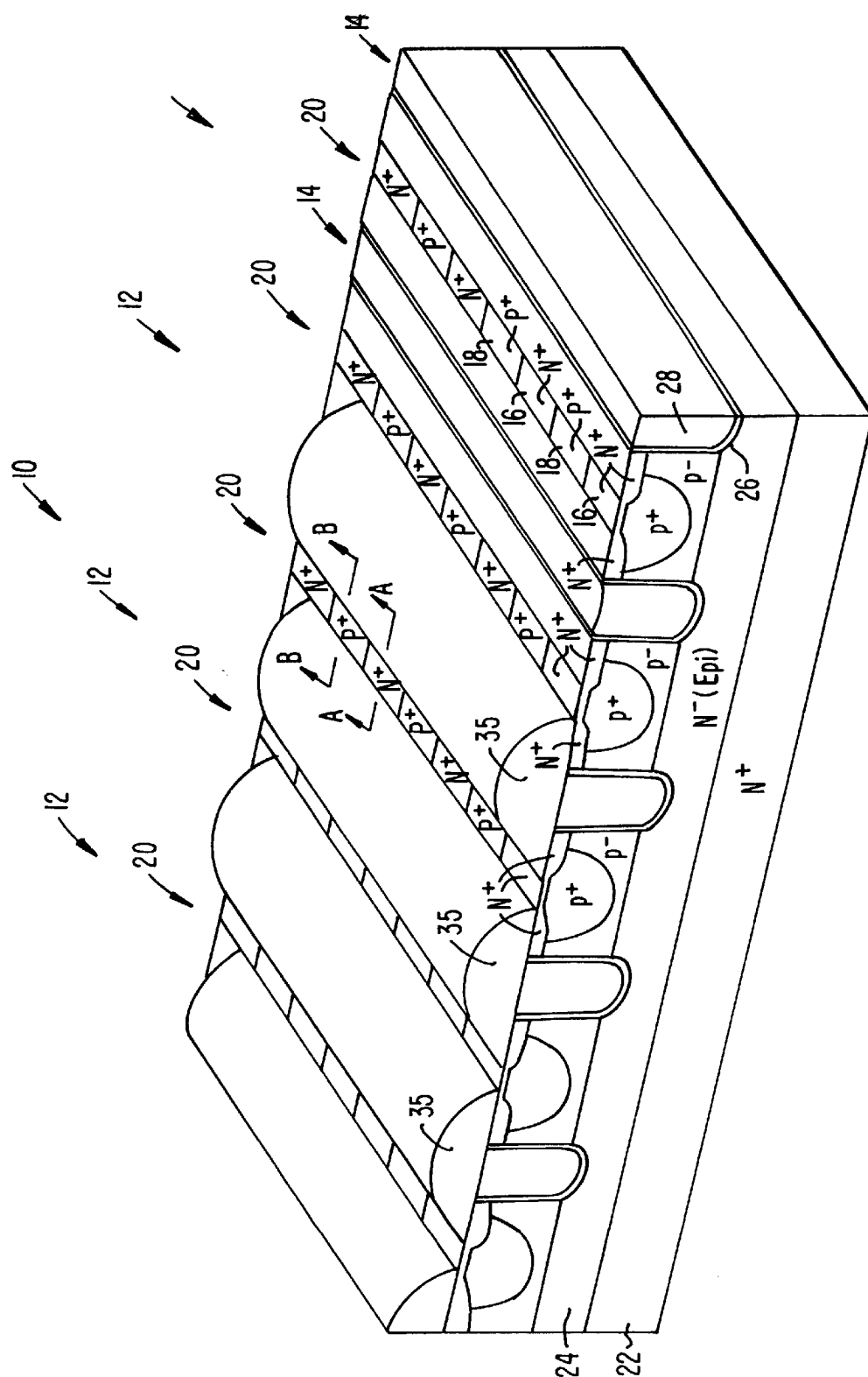


FIG. 1.

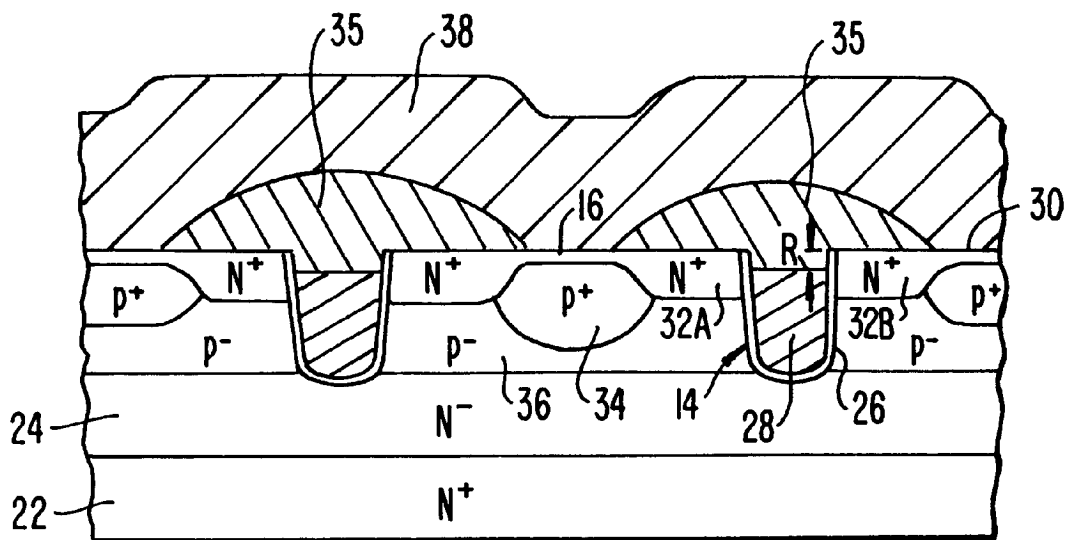


FIG. 1A.

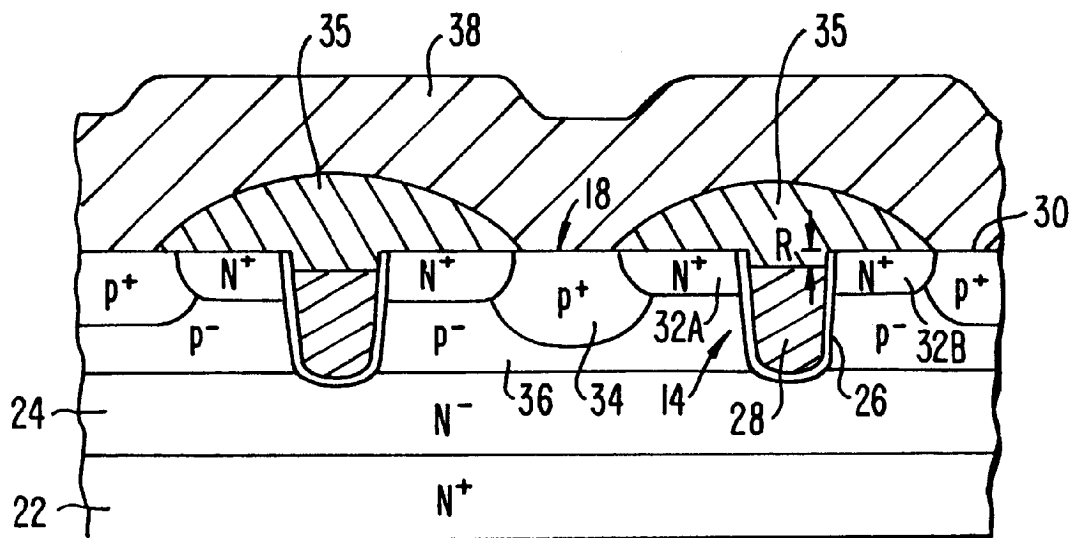


FIG. 1B.

U.S. Patent

Mar. 23, 2004

Sheet 3 of 9

US 6,710,406 B2

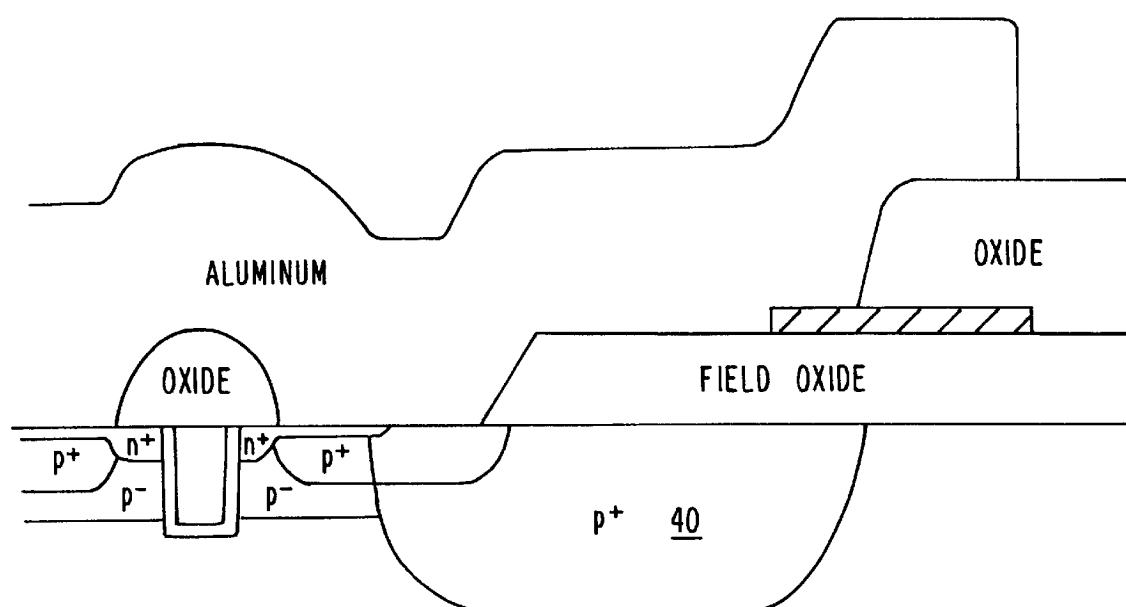


FIG. 2.

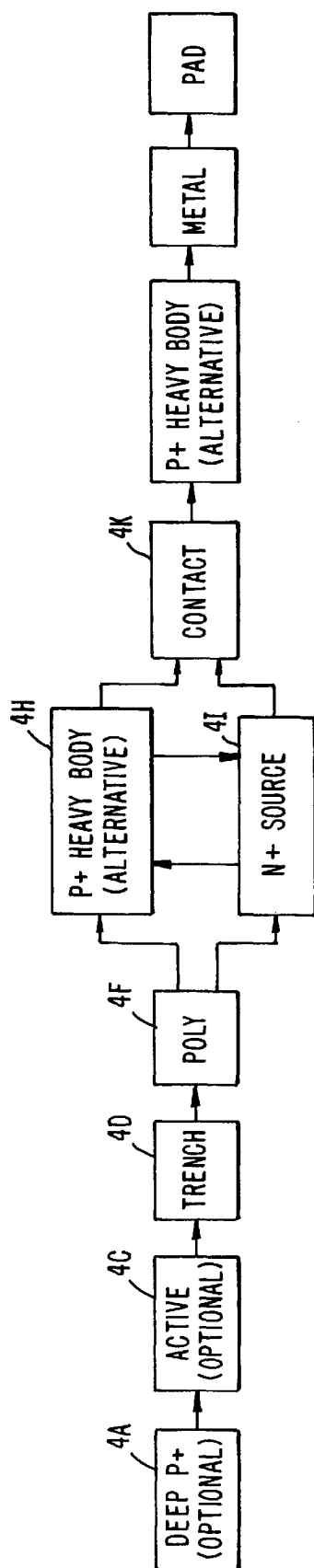


FIG. 3.

U.S. Patent

Mar. 23, 2004

Sheet 5 of 9

US 6,710,406 B2

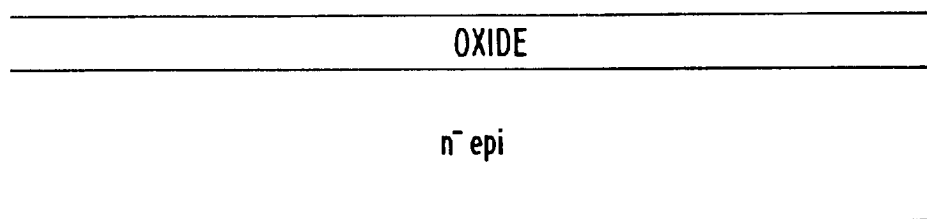


FIG. 4.

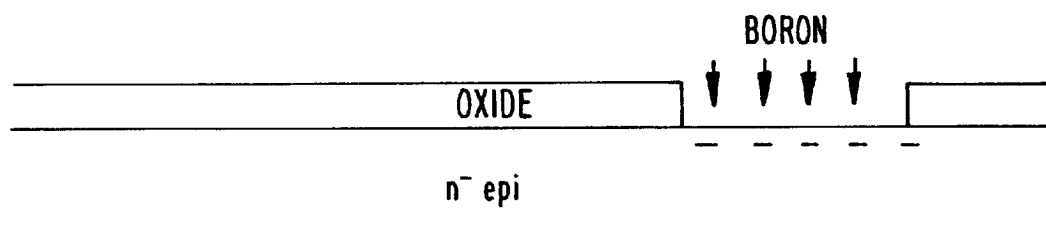


FIG. 4A.

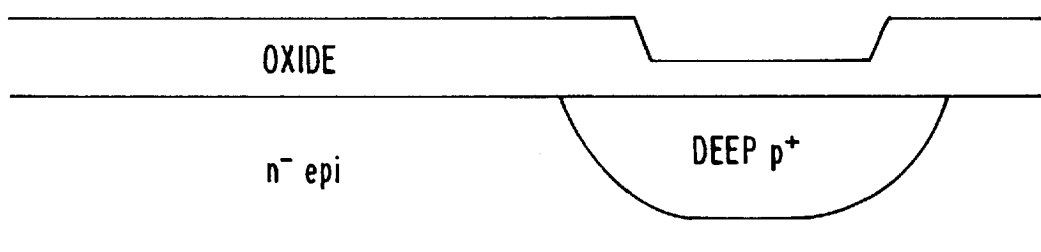


FIG. 4B.

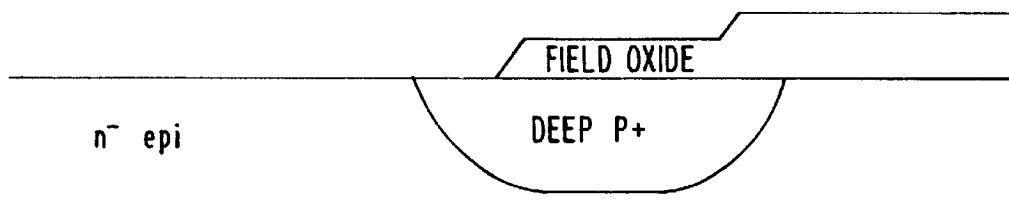


FIG. 4C.

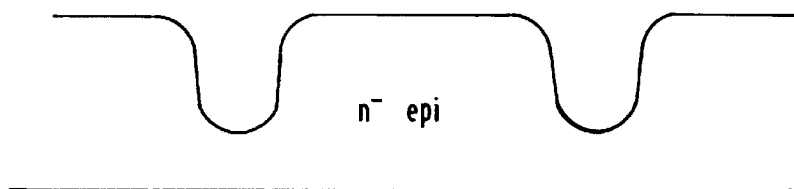


FIG. 4D.

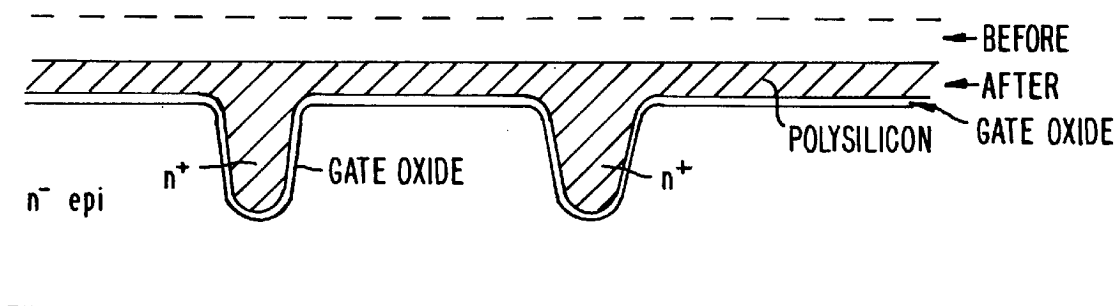


FIG. 4E.

U.S. Patent

Mar. 23, 2004

Sheet 7 of 9

US 6,710,406 B2

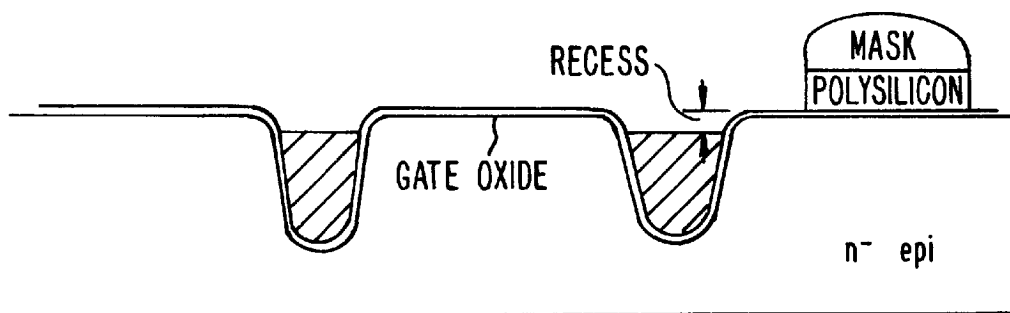


FIG. 4F.

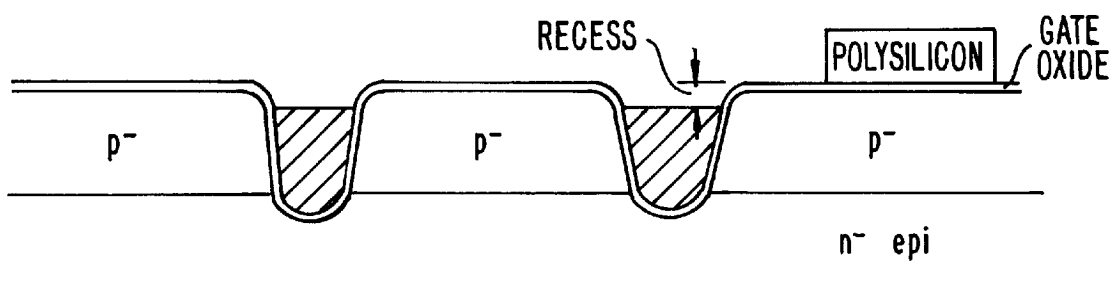


FIG. 4G.

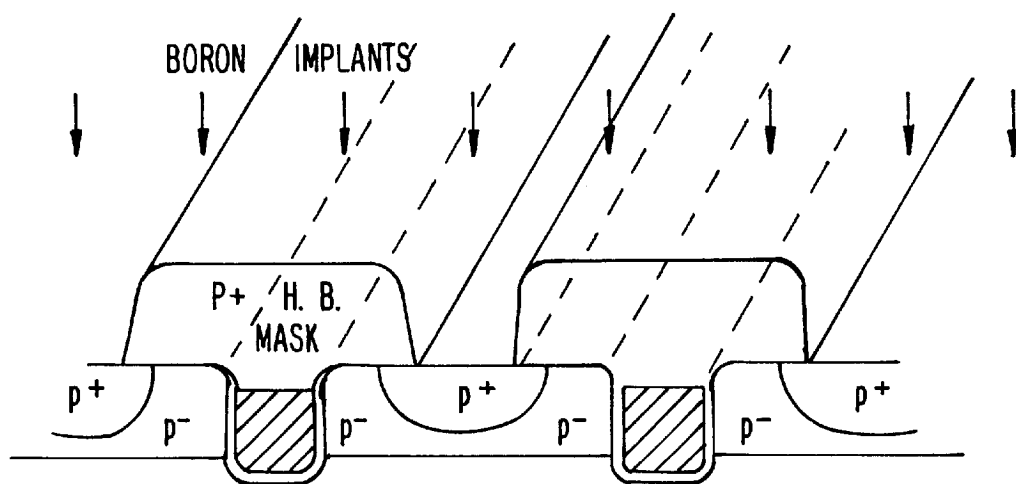


FIG. 4H.

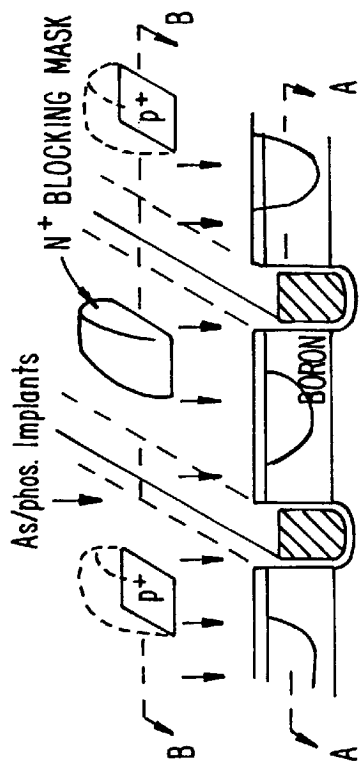
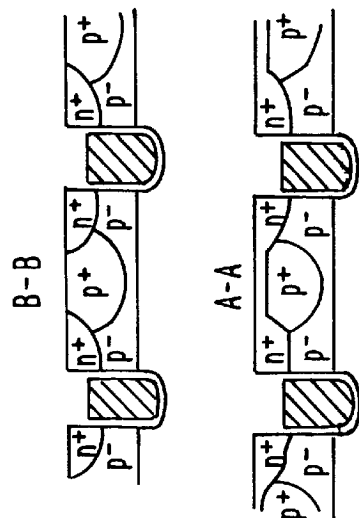


FIG. 4I.



BORON IMPLANTS (ALTERNATIVE)

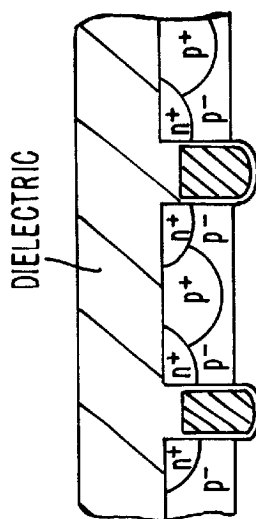


FIG. 4J.

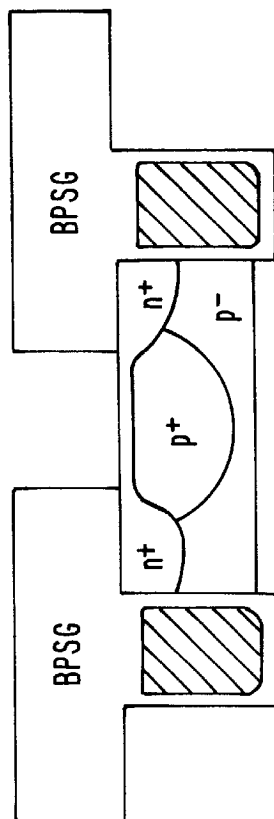


FIG. 4K.

U.S. Patent

Mar. 23, 2004

Sheet 9 of 9

US 6,710,406 B2

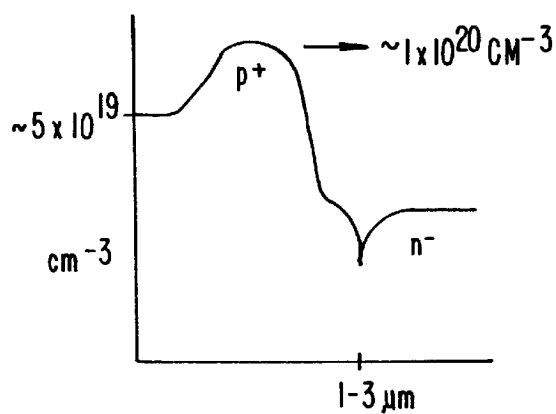


FIG. 5.

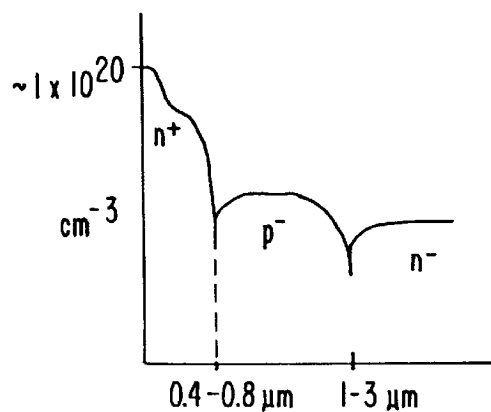


FIG. 5A.

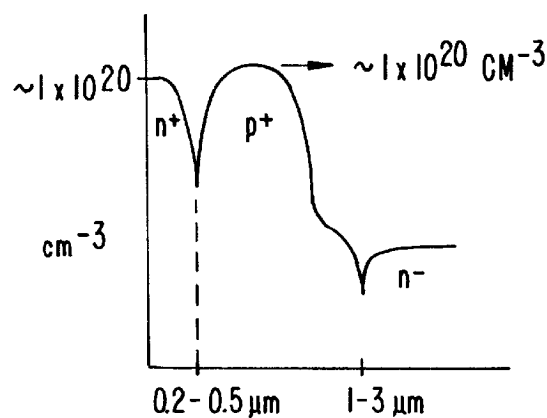


FIG. 5B.

US 6,710,406 B2

1

**FIELD EFFECT TRANSISTOR AND
METHOD OF ITS MANUFACTURE**

This application is a continuation of and claims the benefit of U.S. application Ser. No. 08/970,221 filed Nov. 14, 1997 U.S. Pat. No. 6,429,481, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

The present invention relates to field effect transistors, in particular trench DMOS transistors, and methods of their manufacture.

Power field effect transistors, e.g., MOSFETs (metal oxide semiconductor field effect transistors), are well known in the semiconductor industry. One type of MOSFET is a DMOS (double diffused metal oxide semiconductor) transistor. DMOS transistors typically include a substrate on which an epitaxial layer is grown, a doped source junction, a doped heavy body, a doped well of the same (p or n) doping as the heavy body, and a gate electrode. In trench DMOS transistors the gate electrode is a vertical trench. The heavy body is typically diffused deeper than the bottom of the trench, to minimize electric field at the bottom corners of the trench and thereby prevent avalanche breakdown from damaging the device. The trench is filled with conductive polysilicon, and the polysilicon is generally overetched, to assure that it is completely removed from the surface surrounding the trench. This overetching generally leaves a recess between the top of the polysilicon and the surface of the semiconductor substrate (i.e., the surface of the epitaxial layer). The depth of this recess must be carefully controlled so that it is shallower than the depth of the source junctions. If the recess is deeper than the source junctions the source may miss the gate, resulting in high on-state resistance, high threshold, and potentially a non-functional transistor.

The source and drain junctions can be doped with either p-type or n-type dopants; in either case, the body will be doped with the opposite dopant, e.g., for n-type source and drain the body will be p-type. DMOS transistors in which the source and drain are doped with p-type carriers are referred to as "p-channel". In p-channel DMOS transistors a negative voltage applied to the transistor gate causes current flow from the source region, through a channel region of the body, an accumulation region of the epitaxial layer, and the substrate, to the drain region. Conversely, DMOS transistors, in which the source and drain are doped with n-type carriers, are referred to as "n-channel". In n-channel DMOS transistors a positive voltage applied to the transistor gate causes current to flow from drain to source.

It is desirable that DMOS transistors have low source to drain resistance ($R_{ds(on)}$) when turned on and low parasitic capacitance. The transistor structure should also avoid "punchthrough". Punchthrough occurs when, upon application of a high drain to source voltage, depletion into the body region extends to the source region, forming an undesirable conductive path through the body region when the transistor should be off. Finally, the transistor should have good "ruggedness", i.e., a high activation current is needed to turn on the parasitic transistor that inherently exists in DMOS transistors.

Generally a large number of MOSFET cells are connected in parallel forming a single transistor. The cells may be arranged in a "closed cell" configuration, in which the trenches are laid out in a grid pattern and the cells are enclosed on all sides by trench walls. Alternatively, the cells may be arranged in an "open cell" configuration, in which

2

the trenches are laid out in a "stripe" pattern and the cells are only enclosed on two sides by trench walls. Electric field termination techniques are used to terminate junctions (doped regions) at the periphery (edges) of the silicon die on which the transistors are formed. This tends to cause the breakdown voltage to be higher than it would otherwise be if controlled only by the features of the active transistor cells in the central portions of the die.

SUMMARY OF THE INVENTION

The present invention provides field effect transistors that have an open cell layout that provides good uniformity and high cell density and that is readily scalable. Preferred trench DMOS transistors exhibit low $R_{ds(on)}$, low parasitic capacitance, excellent reliability, resistance to avalanche breakdown degradation, and ruggedness. Preferred devices also include a field termination that enhances resistance to avalanche breakdown. The invention also features a method of making trench DMOS transistors.

In one aspect, the invention features a trench field effect transistor that includes

(a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of the heavy body region relative to the depths of the well and the trench is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped well has a depth less than the predetermined depth of the trench. The trench has rounded top and bottom corners. There is an abrupt junction at the interface between the heavy body and the well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface.

In another aspect, the invention features an array of transistor cells. The array includes (a) a semiconductor substrate, (b) a plurality of gate-forming trenches arranged substantially parallel to each other and extending in a first direction, the space between adjacent trenches defining a contact area, each trench extending a predetermined depth into said substrate, the predetermined depth being substantially the same for all of said gate-forming trenches; (c) surrounding each trench, a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, (d) positioned between each pair of gate-forming trenches, a doped heavy body positioned adjacent each source junction, the deepest portion of each said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches, (e) a doped well surrounding each heavy body beneath the heavy body; and (f) p+ and n+ contacts disposed at the surface of the semiconductor substrate and arranged in alternation along the length of the contact area.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of each heavy body region relative to the depths of the wells and the gate-forming trenches is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped wells

US 6,710,406 B2

3

have a depth less than the predetermined depth of the trenches. The trenches have rounded top and bottom corners. There is an abrupt junction at the interface between each heavy body and the corresponding well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface. The array also includes a field termination structure surrounding the periphery of the array. The field termination structure includes a well having a depth greater than that of the gate-forming trenches. The field termination structure includes a termination trench extending continuously around the periphery of the array, more preferably a plurality of concentrically arranged termination trenches.

In yet another aspect, the invention features a semiconductor die that includes (a) a plurality of DMOS transistor cells arranged in an array on a semiconductor substrate, each DMOS transistor cell including a gate-forming trench, each of said gate-forming trenches having a predetermined depth, the depth of all of the gate-forming trenches being substantially the same; and (b) surrounding the periphery of the array, a field termination structure that extends into the semiconductor substrate to a depth that is deeper than said predetermined depth of said gate-forming trenches.

Preferred embodiments include one or more of the following features. The field termination structure includes a doped well. The field termination structure includes a termination trench. The field termination structure includes a plurality of concentrically arranged termination trenches. Each of the DMOS transistor cells further comprises a doped heavy body and the doped heavy body extends into the semiconductor substrate to a depth that is less than the predetermined depth of the gate-forming trenches.

The invention also features a method of making a heavy body structure for a trench DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into said region a second dopant at a second energy and dosage, said second energy and dosage being relatively less than said first energy and dosage.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$. The second energy is from about 20 to 40 keV. The second dosage is from about $1\text{E}14$ to $1\text{E}15\text{ cm}^{-2}$.

Additionally, the invention features a method of making a source for a trench DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into the region a second dopant at a second energy and dosage, the second energy and dosage being relatively less than the first energy and dosage.

Preferred embodiments include one or more of the following features. The first dopant comprises arsenic and the second dopant comprises phosphorus. The first energy is from about 80 to 120 keV. The first dosage is from about $5\text{E}15$ to $1\text{E}16\text{ cm}^{-2}$. The second energy is from about 40 to 70 keV. The second dosage is from about $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$. The resulting depth of the source is from about 0.4 to $0.8\text{ }\mu\text{m}$ the finished DMOS transistor.

In another aspect, the invention features a method of manufacturing a trench field effect transistor. The method includes (a) forming a field termination junction around the perimeter of a semiconductor substrate, (b) forming an epitaxial layer on the semiconductor substrate, (c) patterning

4

and etching a plurality of trenches into the epitaxial layer; (d) depositing polysilicon to fill the trenches, (e) doping the polysilicon with a dopant of a first type, (f) patterning the substrate and implanting a dopant of a second, opposite type to form a plurality of wells interposed between adjacent trenches, (g)

patterning the substrate and implanting a dopant of the second type to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned above the wells, each heavy body having an abrupt junction with the corresponding well, (h) patterning the substrate and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and (i) applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas.

Other features and advantages of the invention will be apparent from the following detailed description, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a highly enlarged, schematic perspective cross-sectional view showing a portion of a cell array including a plurality of DMOS transistors according to one aspect of the invention. The source metal layer and a portion of the dielectric layer have been omitted to show the underlying layers. FIGS. 1a and 1b are side cross-sectional views of a single line of transistors from the array of FIG. 1, taken along lines A—A and B—B, respectively. In FIGS. 1a and 1b the source metal and dielectric layers are shown.

FIG. 2 is a highly enlarged schematic side cross-sectional view of a semiconductor die showing a portion of the cell array and the field termination.

FIG. 3 is a flow diagram showing the photo mask sequence of a preferred process for forming a trench DMOS transistor of FIG. 1.

FIGS. 4-4k are schematic side cross-sectional views showing the individual steps of the process diagrammed in FIG. 3. The figure numbers for the detailed views in FIGS. 4-4k are shown parenthetically under the corresponding diagram boxes in FIG. 3.

FIGS. 5, 5a and 5b are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A cell array 10, including a plurality of rows 12 of trench DMOS transistors, is shown in FIG. 1. Cell array 10 has an open cell configuration, i.e., trenches 14 run in only one direction, rather than forming a grid. Individual cells are formed by alternating n+ source contacts 16 and p+ contacts 18 in rows 20 that run parallel to and between trenches 14. The configuration of the regions of each row that have an n+ source contact are shown in cross-section in FIG. 1a, while the regions that have a p+ contact are shown in FIG. 1b.

As shown in FIGS. 1a and 1b, each trench DMOS transistor includes a doped n+ substrate (drain) layer 22, a more lightly doped n- epitaxial layer 24, and a gate electrode 28. Gate electrode 28 comprises a conductive polysilicon that fills a trench 14. A gate oxide 26 coats the walls of the trench and underlies the polysilicon. The top surface of the polysilicon is recessed from the surface 30 of the semiconductor substrate by a distance R (typically from about 0 to $0.4\text{ }\mu\text{m}$). N+ doped source regions 32a, 32b are

US 6,710,406 B2

5

positioned one on each side of the trench **14**. A dielectric layer **35** covers the trench opening and the two source regions **32a**, **32b**. Extending between the source regions of adjacent cells is a p+ heavy body region **34** and, beneath it, a flat-bottomed p- well **36**. In the areas of the cell array which have a n+ contact **16**, a shallow n+ doped contact region extends between the n+ source regions. A source metal layer **38** covers the surface of the cell array.

The transistor shown in FIGS. **1a** and **1b** includes several features that enhance the ruggedness of the transistor and its resistance to avalanche breakdown degradation.

First, the depth of the p+ heavy body region **34** relative to the depths of the trench **14** and the flat bottom of the p- well is selected so that the peak electric field when voltage is applied to the transistor will be approximately halfway between adjacent trenches. The preferred relative depths of the p+ heavy body, the p- well and the trench are different for different device layouts. However, preferred relative depths can be readily determined empirically (by observing the location of peak electric field) or by finite element analysis.

Second, the bottom corners of the trench **14** are rounded (preferably, the top corners are also rounded; this feature is not shown). Corner rounding can be achieved using the process described in copending application U.S. Ser. No. 08/959,197, filed on Oct. 28, 1997. The rounded corners of the trench also tend to cause the peak electric field to be moved away from the trench corners and towards a central location between adjacent trenches.

Third, an abrupt junction at the interface between the p+ heavy body and the p- well causes the peak electric field to occur in that area of the interface. Avalanche multiplication initiates at the location of the peak electric field, thus steering hot carriers away from the sensitive gate oxide and channel regions. As a result, this structure improves reliability and avalanche ruggedness without sacrificing cell density as much as a deeper heavy body junction. This abrupt junction can be achieved by the double doping process that will be described below, or by other processes for forming abrupt junctions, many of which are known in the semiconductor field.

Lastly, referring to FIG. **2**, the cell array is surrounded by a field termination junction **40** which increases the breakdown voltage of the device and draws avalanche current away from the cell array to the periphery of the die. Field termination junction **40** is a deep p+ well, preferably from about 1 to 3 μm deep at its deepest point, that is deeper than the p+ heavy body regions **34** in order to reduce the electric field caused by the junction curvature. A preferred process for making the above-described transistors is shown as a flow diagram in FIG. **3**, and the individual steps are shown schematically in FIGS. **4-4k**. It is noted that some steps that are conventional or do not require illustration are described below but not shown in FIGS. **4-4k**. As indicated by the arrows in FIG. **3**, and as will be discussed below, the order of the steps shown in FIGS. **4-4k** can be varied. Moreover, some of the steps shown in FIGS. **4-4k** are optional, as will be discussed.

A semiconductor substrate is initially provided. Preferably, the substrate is a N++ Si substrate, having a standard thickness, e.g., 500 μm , and a very low resistivity, e.g., 0.001 to 0.005 Ohm-cm. An epitaxial layer is deposited onto this substrate, as is well known, preferably to a thickness of from about 4 to 10 μm . Preferably the resistivity of the epitaxial layer is from about 0.1 to 3.0 Ohm-cm.

Next, the field termination junction **40** is formed by the steps shown in FIGS. **4-4c**. In FIG. **4**, an oxide layer is

6

formed on the surface of the epitaxial layer. Preferably, the thickness of the oxide is from about 5 to 10 kÅ. Next, as shown in FIG. **4a**, the oxide layer is patterned and etched to define a mask, and the p+ dopant is introduced to form the deep p+ well field termination. A suitable dopant is boron, implanted at an energy of from about 40 to 100 keV and a dose of $1\text{E}14$ (1×10^{14}) to $1\text{E}16$ cm^{-2} . As shown in FIG. **4b**, the p+ dopant is then driven further into the substrate, e.g., by diffusion, and a field oxide layer is formed over the p+ junction. Preferably the oxide thickness is from about 4 to 10 kÅ. Finally, the oxide (FIG. **4**) over the active area of the substrate (the area where the cell array will be formed) is patterned and removed by any suitable etching process, leaving only the field oxide in suitable areas. This leaves the substrate ready for the following steps that will form the cell array.

It is noted that, as an alternative to steps **4-4c**, a suitable field termination structure can be formed using a ring-shaped trench which surrounds the periphery of the cell array and acts to lessen the electric field and increase the resistance to avalanche breakdown degradation. This trench field termination does not require a field oxide or deep p+ body junction to be effective. Consequently, it can be used to reduce the number of process steps. Using a trench ring (or multiple concentric trench rings) to form a field termination is described in, e.g., U.S. Pat. No. 5,430,324, the full disclosure of which is hereby incorporated herein by reference. Preferably, the trench would have substantially the same depth as the trenches in the cell array.

The cell array is formed by the steps shown in FIGS. **4d-4k**. First, a plurality of trenches are patterned and etched into the epitaxial layer of the substrate (FIG. **4d**). Preferably, as noted above, the trenches are formed using the process U.S. Application No. Ser. 08/959,197, filed on Oct. 28, 1997, now U.S. Pat. No. 6,103,635, so that the upper and lower corners of each trench will be smoothly rounded. As shown in FIG. **1** and described above, the trenches are patterned to run in only one direction, defined as an open cell structure. After trench formation, a gate oxide layer is formed on the trench walls, as is well known in the semiconductor field. Preferably the gate oxide has a thickness of from about 100 to 800 Å.

Next, as shown in FIG. **4e**, polysilicon is deposited to fill the trench and cover the surface of the substrate, generally to a thickness of from about 1 to 2 μm depending on the trench width (shown by the dotted lines in FIG. **4e**). This layer is then planarized by the nature of its thickness relative to the trench width, typically from about 2 to 5 kÅ (indicated by solid lines in FIG. **4e**). The polysilicon is then doped to n-type, e.g., by conventional POCL₃ doping or by phosphorus implant. The backside of the wafer need not be stripped (as is conventionally done prior to doping the polysilicon to enhance defect gettering) because any further doping of the highly doped substrate would be unlikely to result in any enhancement in defect gettering.

The polysilicon is then patterned with a photoresist mask and etched to remove it from the trench areas, as shown in FIG. **4f**. A small recess between the top of the polysilicon in the trench and the substrate surface inherently results when the polysilicon is etched completely to remove all of the polysilicon from the substrate surface. The depth of this recess must be controlled so that it does not exceed the depth of the n+ source junction that will be formed in a later step. To reduce the need to carefully control this aspect of the process, a relatively deep n+ source junction is formed, as will be discussed below.

Then, as shown in FIG. **4g**, the p- well is formed by implanting the dopant, e.g., a boron implant at an energy of

US 6,710,406 B2

7

30 to 100 keV and a dosage of $1\text{E}13$ to $1\text{E}15$, and driving it in to a depth of from about 1 to 3 μm using conventional drive in techniques.

The next two steps (p+ heavy body formation) can be performed either before formation of the n+ source junction, or afterwards, as indicated by the arrows in FIG. 3. P+ heavy body formation and n+ source junction formation can be performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. 4h. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. 4k, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p- well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$, and a second boron implant at an energy of 20 to 40 keV and a dose of $1\text{E}14$ to $1\text{E}15\text{ cm}^{-2}$. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact 18. The resulting p+ heavy body junction is preferably about 0.4 to 1 μm deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5 μm deep), and includes a region of high dopant concentration near the interface with the p-well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. 5.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts 18 (FIGS. 1 and 1b), as shown in FIG. 4i. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. 4l, which correspond to FIGS. 1a and 1b).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of $5\text{E}15$ to $1\text{E}16\text{ cm}^{-2}$ followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$. The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source

8

regions will have a depth of about 0.4 to 0.8 μm after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts 16 (see FIGS. 1 and 1a) by compensating (converting) the p-type surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. 5a and 5b, respectively.

Thus, the alternating p+ and n+ contacts 18, 16, shown in FIG. 1 are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower $R_{ds, on}$.

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900°C ., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. 4j), after which the dielectric is patterned and etched (FIG. 4k) to define electrical contact openings over the n+ and p+ contacts 16, 18.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well known in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "n" doped instead, and vice versa.

What is claimed is:

1. A trench field effect transistor comprising:

- a semiconductor substrate having dopants of a first conductivity type;
- a trench extending to a first depth into said semiconductor substrate;
- a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;
- a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and
- a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;

wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.

US 6,710,406 B2

9

2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.

3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.

4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.

5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.

6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.

7. The trenched field effect transistor of claim 1 further comprising a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fourth depth that is deeper than said first depth of the trench.

8. The trenched field effect transistor of claim 7 wherein said deep doped region forms a PN junction diode with the substrate.

9. The trenched field effect transistor of claim 7 wherein the deep doped region forms a termination structure.

10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.

11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.

12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.

13. A field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending to a first depth into said substrate, the space between adjacent trenches defining a contact area;

a pair of doped source junctions positioned on opposite sides of each trench, the source junctions having dopants of the first conductivity type;

a doped well having dopants of a second conductivity type with a charge opposite that of the first conductivity type, the doped well being formed in the semiconductor substrate between each pair of gate-forming trenches;

a heavy body formed inside the doped well and having a second depth that is less than the first depth of the trenches; and

heavy body contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction with the well, and the depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.

14. The field effect transistor of claim 13, wherein each said doped well has a substantially flat bottom.

15. The field effect transistor of claim 13 wherein the adjusted depth of the junction causes the breakdown origi-

10

nation point to occur approximately halfway between adjacent gate-forming trenches.

16. The field effect transistor of claim 13 wherein each said doped well has a depth less than the first depth of said gate-forming trenches.

17. The field effect transistor of claim 13 wherein each said gate-forming trench has rounded top and bottom corners.

18. The field effect transistor of claim 13 further comprising a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a depth greater than said first depth of the said plurality of gate-forming trenches.

19. The field effect transistor of claim 18 wherein the deep doped region forms a PN junction diode with the substrate.

20. The field effect transistor of claim 19 wherein the deep doped region forms a field termination structure surrounding the periphery of the plurality of gate-forming trenches.

21. The field effect transistor of claim 20 further comprising:

a layer of dielectric material formed over the deep doped region; and

a layer of conductive material formed on top of the layer of dielectric material.

22. The field effect transistor of claim 13 further comprising a field termination structure including a termination trench extending continuously around the periphery of the plurality of gate-forming trenches.

23. The field effect transistor of claim 22 wherein said field termination structure comprises a plurality of concentrically arranged termination trenches.

24. The field effect transistor of claim 13 wherein the heavy body forms a continuous doped region along substantially the entire length of said contact area.

25. The field effect transistor of claim 13 wherein said doped source regions extend along the length of the trench.

26. The field effect transistor of claim 25 further comprising a source contact region defined at the surface of the semiconductor substrate and configured to contacting the doped source regions.

27. The field effect transistor of claim 25 further comprising a plurality of source contact regions disposed along the length of the contact area in an alternating fashion with the plurality of heavy body contact regions.

28. The field effect transistor of claim 13 wherein between a pair of adjacent trenches, the heavy body is bounded by the pair of adjacent trenches and the doped source regions.

29. The field effect transistor of claim 13 wherein between a pair of adjacent trenches, the heavy body extends continuously parallel to the longitudinal axis of the trenches.

30. The field effect transistor of claim 13 further comprising:

a layer of dielectric lining inside walls of each of said plurality of gate-forming trenches; and

a layer of conductive material substantially filling the gate-forming trenches.

31. The field effect transistor of claim 30 wherein the layer of conductive material comprises polysilicon.

32. The field effect transistor of claim 30 wherein the top surface of the layer of conductive material substantially filling the gate-forming trenches is recessed relative to the top surface of the semiconductor substrate.

* * * * *

EXHIBIT C

-

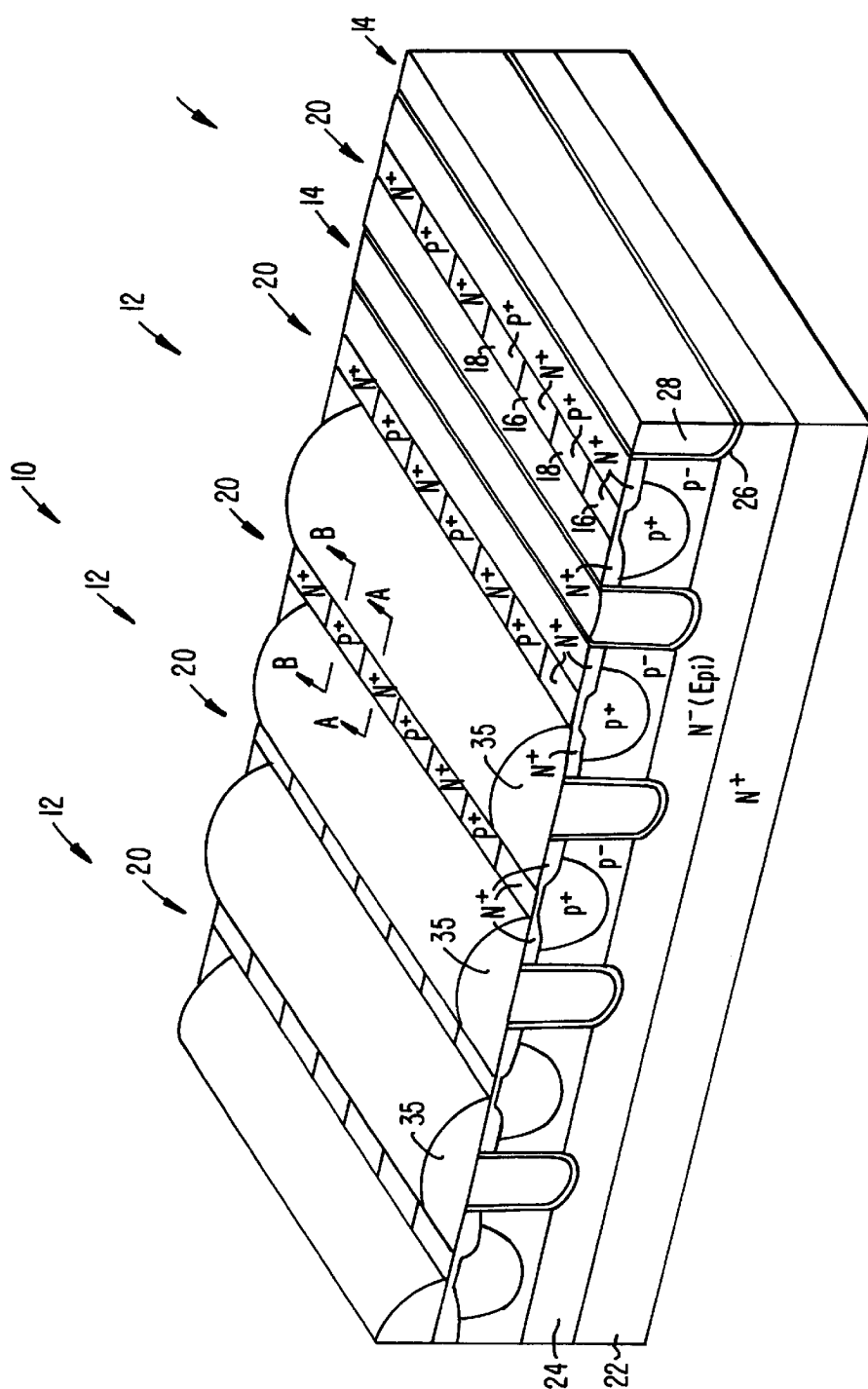


FIG. 1.

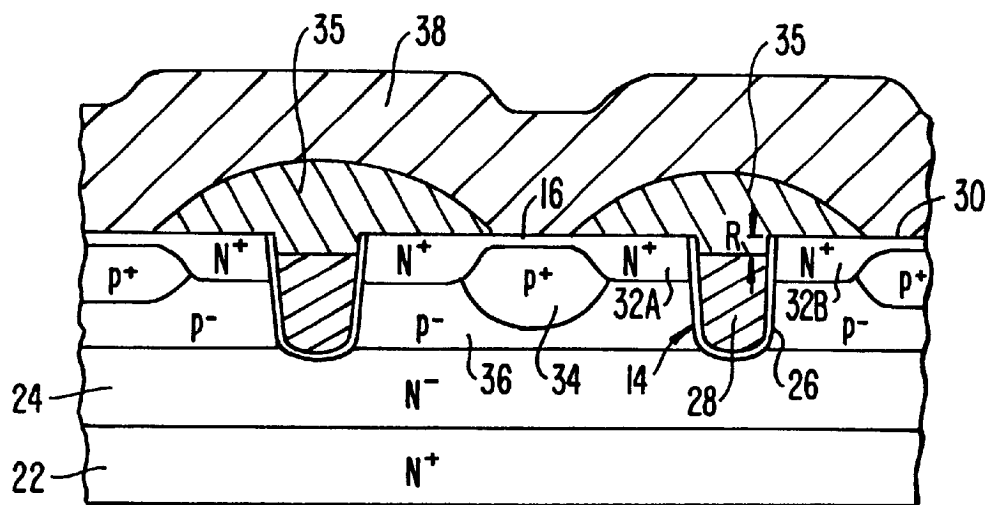


FIG. 1A.

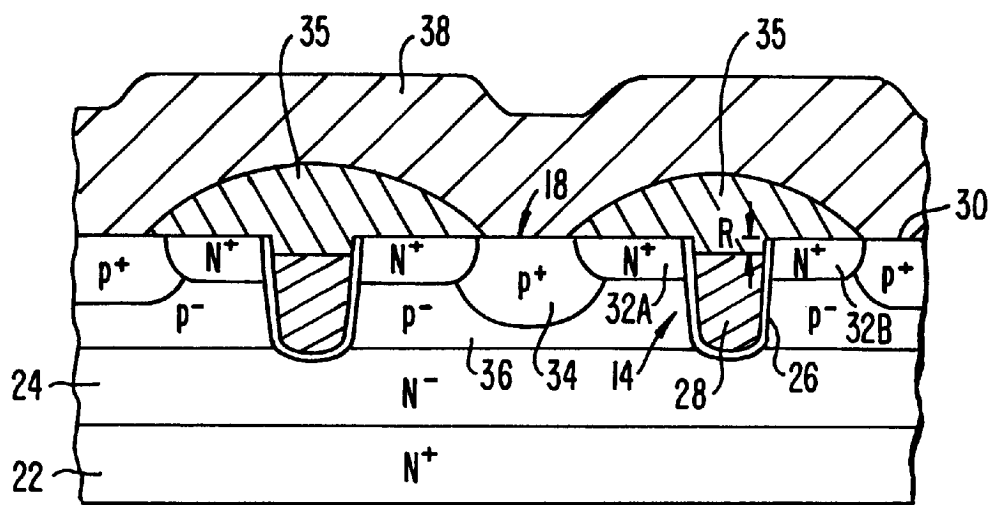


FIG. 1B.

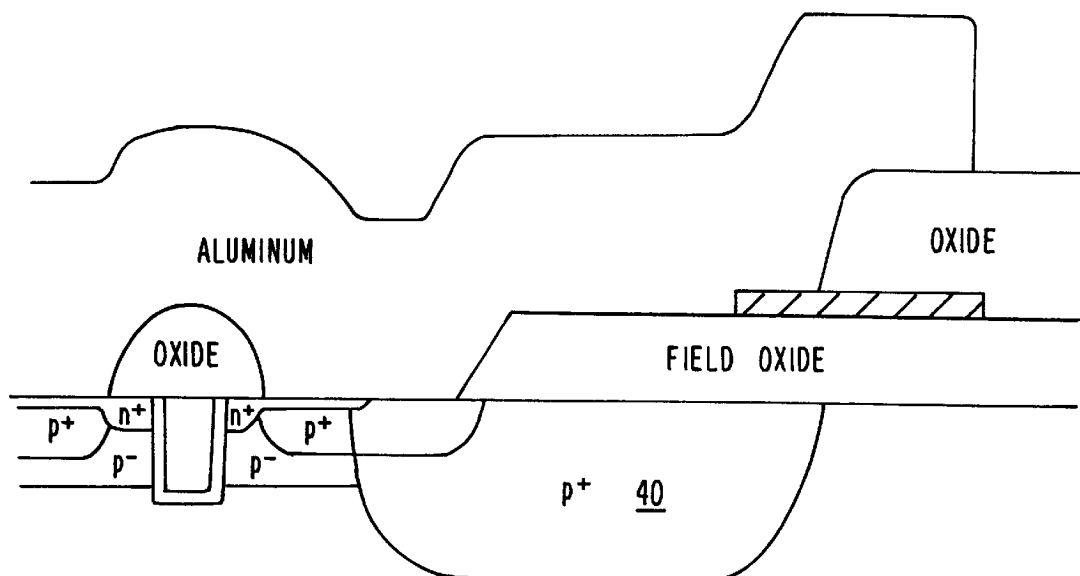


FIG. 2.

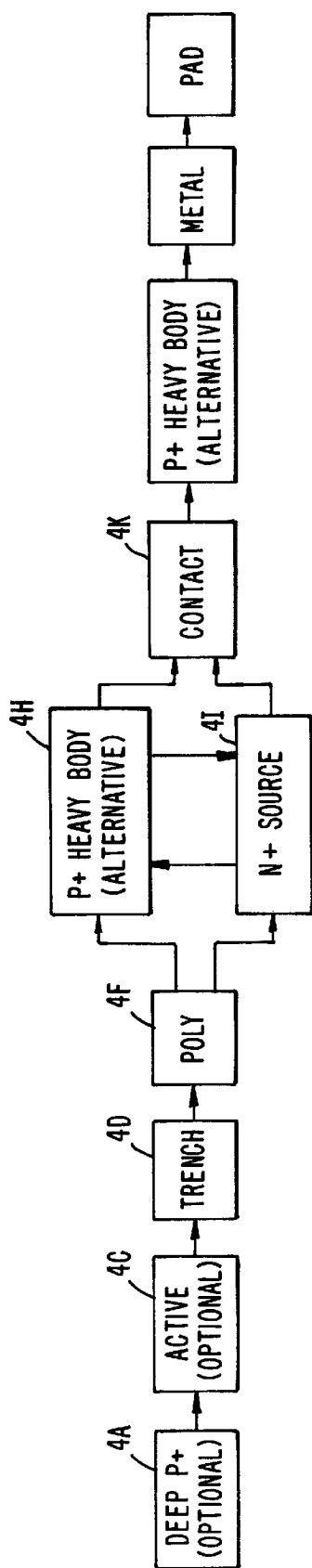


FIG. 3.

U.S. Patent

Feb. 18, 2003

Sheet 5 of 9

US 6,521,497 B2

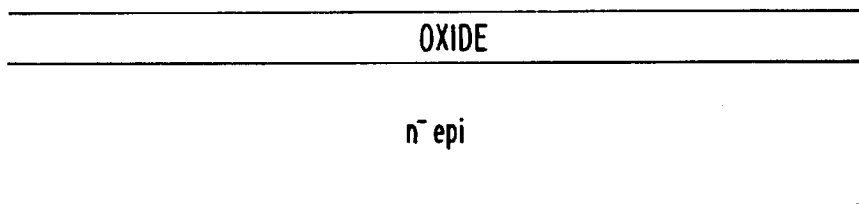


FIG. 4.

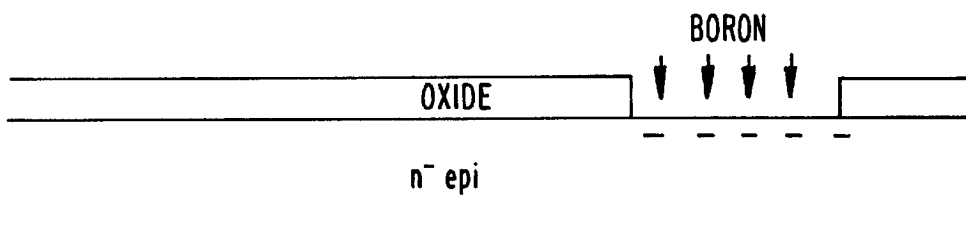


FIG. 4A.

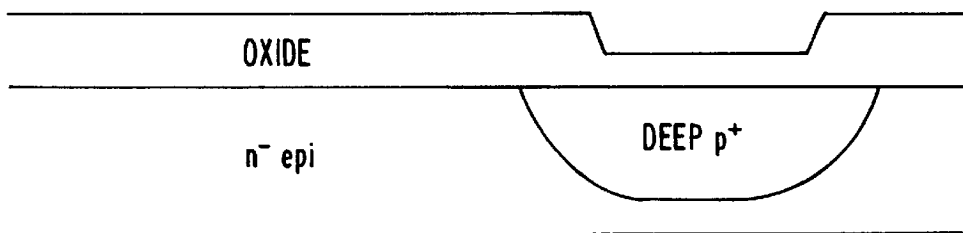


FIG. 4B.

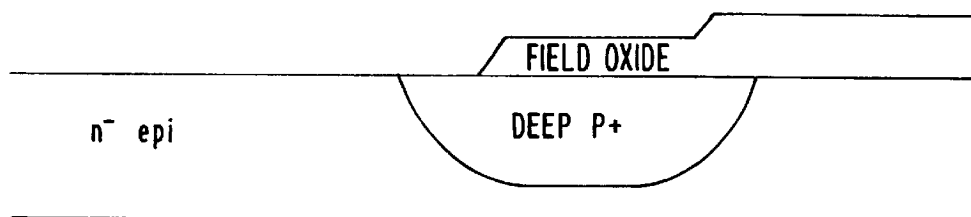


FIG. 4C.

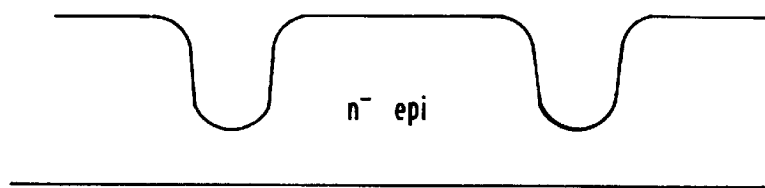


FIG. 4D.

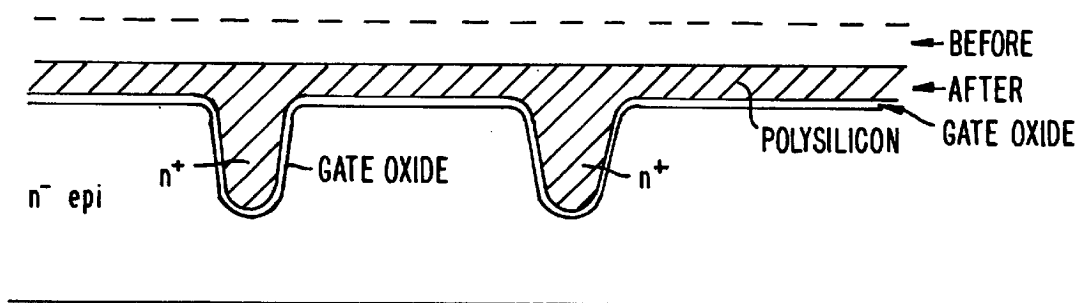


FIG. 4E.

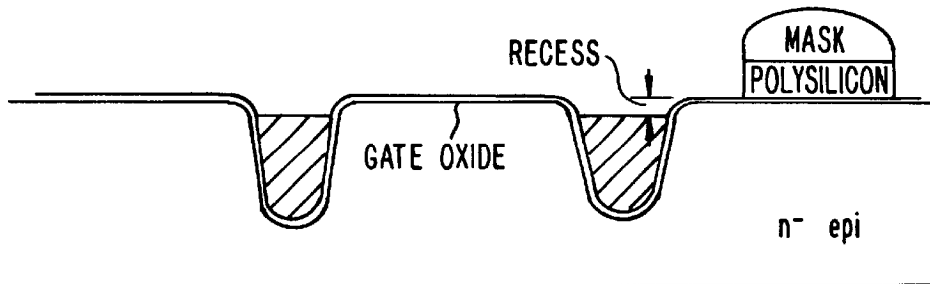


FIG. 4F.

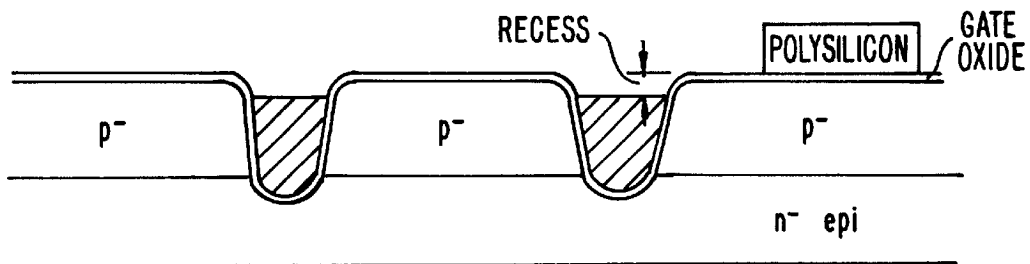


FIG. 4G.

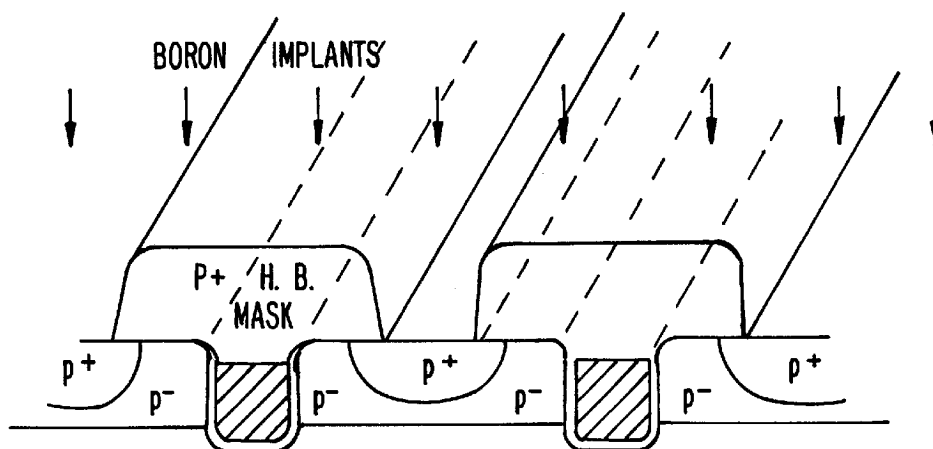


FIG. 4H.

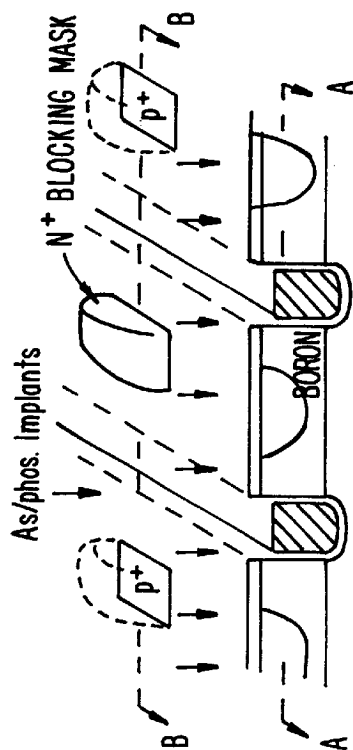


FIG. 4I.

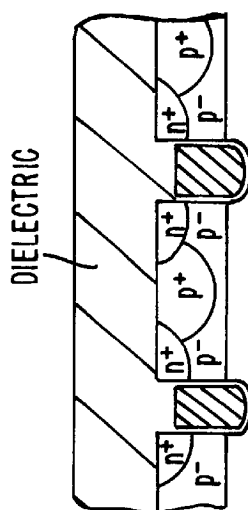
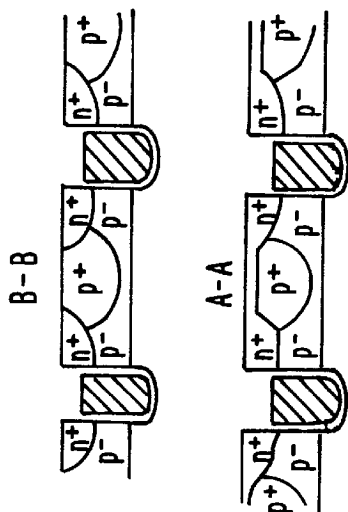


FIG. 4J.

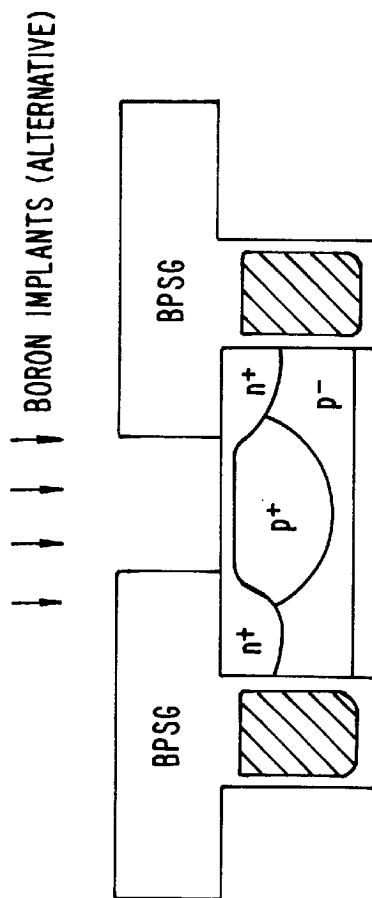


FIG. 4K.

U.S. Patent

Feb. 18, 2003

Sheet 9 of 9

US 6,521,497 B2

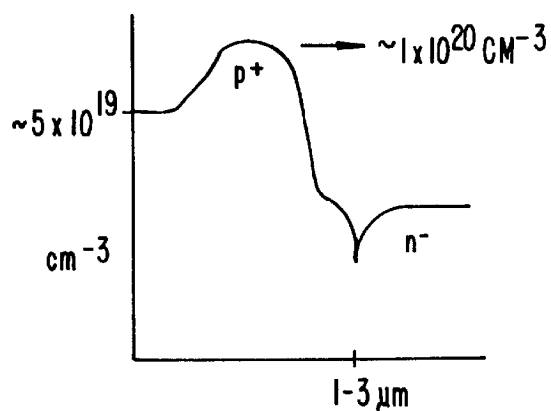


FIG. 5.

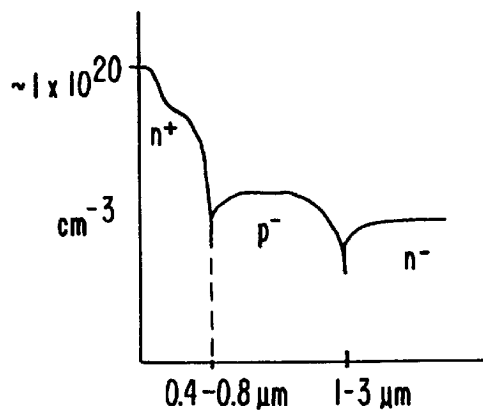


FIG. 5A.

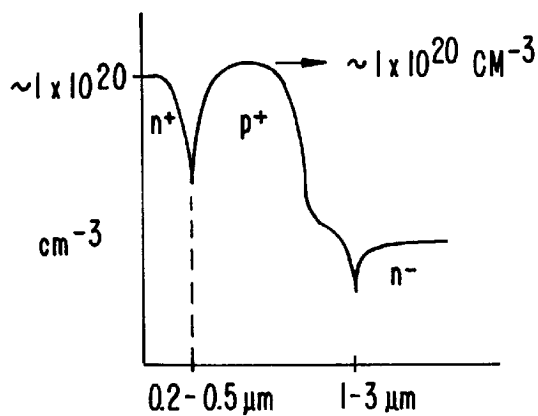


FIG. 5B.

US 6,521,497 B2

1

METHOD OF MANUFACTURING A FIELD EFFECT TRANSISTOR

This application is a division of U.S. application Ser. No. 08/970,221 filed Nov. 14, 1997 now U.S. Pat. No. 6,429,481.

BACKGROUND OF THE INVENTION

The present invention relates to field effect transistors, in particular trench DMOS transistors, and methods of their manufacture.

Power field effect transistors, e.g., MOSFETs (metal oxide semiconductor field effect transistors), are well known in the semiconductor industry. One type of MOSFET is a DMOS (double diffused metal oxide semiconductor) transistor. DMOS transistors typically include a substrate on which an epitaxial layer is grown, a doped source junction, a doped heavy body, a doped well of the same (p or n) doping as the heavy body, and a gate electrode. In trench DMOS transistors the gate electrode is a vertical trench. The heavy body is typically diffused deeper than the bottom of the trench, to minimize electric field at the bottom corners of the trench and thereby prevent avalanche breakdown from damaging the device. The trench is filled with conductive polysilicon, and the polysilicon is generally overetched, to assure that it is completely removed from the surface surrounding the trench. This overetching generally leaves a recess between the top of the polysilicon and the surface of the semiconductor substrate (i.e., the surface of the epitaxial layer). The depth of this recess must be carefully controlled so that it is shallower than the depth of the source junctions. If the recess is deeper than the source junctions the source may miss the gate, resulting in high on-state resistance, high threshold, and potentially a non-functional transistor.

The source and drain junctions can be doped with either p-type or n-type dopants; in either case, the body will be doped with the opposite dopant, e.g., for n-type source and drain the body will be p-type. DMOS transistors in which the source and drain are doped with p-type carriers are referred to as "p-channel". In p-channel DMOS transistors a negative voltage applied to the transistor gate causes current flow from the source region, through a channel region of the body, an accumulation region of the epitaxial layer, and the substrate, to the drain region. Conversely, DMOS transistors, in which the source and drain are doped with n-type carriers, are referred to as "n-channel". In n-channel DMOS transistors a positive voltage applied to the transistor gate causes current to flow from drain to source.

It is desirable that DMOS transistors have low source to drain resistance ($R_{ds(on)}$) when turned on and low parasitic capacitance. The transistor structure should also avoid "punch through". Punchthrough occurs when, upon application of a high drain to source voltage, depletion into the body region extends to the source region, forming an undesirable conductive path through the body region when the transistor should be off. Finally, the transistor should have good "ruggedness", i.e., a high activation current is needed to turn on the parasitic transistor that inherently exists in DMOS transistors.

Generally a large number of MOSFET cells are connected in parallel forming a single transistor. The cells may be arranged in a "closed cell" configuration, in which the trenches are laid out in a grid pattern and the cells are enclosed on all sides by trench walls. Alternatively, the cells may be arranged in an "open cell" configuration, in which the trenches are laid out in a "stripe" pattern and the cells are only enclosed on two sides by trench walls. Electric field

2

termination techniques are used to terminate junctions (doped regions) at the periphery (edges) of the silicon die on which the transistors are formed. This tends to cause the breakdown voltage to be higher than it would otherwise be if controlled only by the features of the active transistor cells in the central portions of the die.

SUMMARY OF THE INVENTION

The present invention provides field effect transistors that have an open cell layout that provides good uniformity and high cell density and that is readily scalable. Preferred trench DMOS transistors exhibit low $R_{ds(on)}$, low parasitic capacitance, excellent reliability, resistance to avalanche breakdown degradation, and ruggedness. Preferred devices also include a field termination that enhances resistance to avalanche breakdown. The invention also features a method of making trench DMOS transistors.

In one aspect, the invention features a trench field effect transistor that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of the heavy body region relative to the depths of the well and the trench is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped well has a depth less than the predetermined depth of the trench. The trench has rounded top and bottom corners. There is an abrupt junction at the interface between the heavy body and the well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface.

In another aspect, the invention features an array of transistor cells. The array includes (a) a semiconductor substrate, (b) a plurality of gate-forming trenches arranged substantially parallel to each other and extending in a first direction, the space between adjacent trenches defining a contact area, each trench extending a predetermined depth into said substrate, the predetermined depth being substantially the same for all of said gate forming trenches; (c) surrounding each trench, a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, (d) positioned between each pair of gate-forming trenches, a doped heavy body positioned adjacent each source junction, the deepest portion of each said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches, (e) a doped well surrounding each heavy body beneath the heavy body; and (f) p+ and n+ contacts disposed at the surface of the semiconductor substrate and arranged in alternation along the length of the contact area.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of each heavy body region relative to the depths of the wells and the gate-forming trenches is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped wells have a depth less than the predetermined depth of the trenches. The trenches have rounded top and bottom corners.

US 6,521,497 B2

3

There is an abrupt junction at the interface between each heavy body and the corresponding well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface. The array also includes a field termination structure surrounding the periphery of the array. The field termination structure includes a well having a depth greater than that of the gate-forming trenches. The field termination structure includes a termination trench extending continuously around the periphery of the array, more preferably a plurality of concentrically arranged termination trenches.

In yet another aspect, the invention features a semiconductor die that includes (a) a plurality of DMOS transistor cells arranged in an array on a semiconductor substrate, each DMOS transistor cell including a gate-forming trench, each of said gate-forming trenches having a predetermined depth, the depth of all of the gate-forming trenches being substantially the same; and (b) surrounding the periphery of the array, a field termination structure that extends into the semiconductor substrate to a depth that is deeper than said predetermined depth of said gate-forming trenches.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$. The second energy is from about 20 to 40 keV. The second dosage is from about $1\text{E}14$ to $1\text{E}15\text{ cm}^{-2}$.

The invention also features a method of making a heavy body structure for a trench DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into said region a second dopant at a second energy and dosage, said second energy and dosage being relatively less than said first energy and dosage.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about $1\text{E}15$ to $5\text{E}15$. The second energy is from about 20 to 40 keV. The second dosage is from about $1\text{E}14$ to $1\text{E}15$.

Additionally, the invention features a method of making a source for a trench DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into the region a second dopant at a second energy and dosage, the second energy and dosage being relatively less than the first energy and dosage.

Preferred embodiments include one or more of the following features. The first dopant comprises arsenic and the second dopant comprises phosphorus. The first energy is from about 80 to 120 keV. The first dosage is from about $5\text{E}15$ to $1\text{E}16\text{ cm}^{-2}$. The second energy is from about 40 to 70 keV. The second dosage is from about $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$. The resulting depth of the source is from about 0.4 to $0.8\text{ }\mu\text{m}$ the finished DMOS transistor.

In another aspect, the invention features a method of manufacturing a trench field effect transistor. The method includes (a) forming a field termination junction around the perimeter of a semiconductor substrate, (b) forming an epitaxial layer on the semiconductor substrate, (c) patterning and etching a plurality of trenches into the epitaxial layer; (d) depositing polysilicon to fill the trenches, (e) doping the polysilicon with a dopant of a first type, (f) patterning the substrate and implanting a dopant of a second, opposite type

4

to form a plurality of wells interposed between adjacent trenches, (g) patterning the substrate and implanting a dopant of the second type to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned above the wells, each heavy body having an abrupt junction with the corresponding well, (h) patterning the substrate and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and (i) applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas.

Other features and advantages of the invention will be apparent from the following detailed description, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a highly enlarged, schematic perspective cross-sectional view showing a portion of a cell array including a plurality of DMOS transistors according to one aspect of the invention. The source metal layer and a portion of the dielectric layer have been omitted to show the underlying layers. FIGS. 1a and 1b are side cross-sectional views of a single line of transistors from the array of FIG. 1, taken along lines A—A and B—B, respectively. In FIGS. 1a and 1b the source metal and dielectric layers are shown.

FIG. 2 is a highly enlarged schematic side cross-sectional view of a semiconductor die showing a portion of the cell array and the field termination.

FIG. 3 is a flow diagram showing the photo mask sequence of a preferred process for forming a trench DMOS transistor of FIG. 1.

FIGS. 4-4k are schematic side cross-sectional views showing the individual steps of the process diagrammed in FIG. 3. The figure numbers for the detailed views in FIGS. 4-4k are shown parenthetically under the corresponding diagram boxes in FIG. 3.

FIGS. 5 and 5b are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A cell array 10, including a plurality of rows 12 of trench DMOS transistors, is shown in FIG. 1. Cell array 10 has an open cell configuration, i.e., trenches 14 run in only one direction, rather than forming a grid. Individual cells are formed by alternating n+ source contacts 16 and p+ contacts 18 in rows 20 that run parallel to and between trenches 14. The configuration of the regions of each row that have an n+ source contact are shown in cross-section in FIG. 1a, while the regions that have a p+ contact are shown in FIG. 1b.

As shown in FIGS. 1a and 1b, each trench DMOS transistor includes a doped n+ substrate (drain) layer 22, a more lightly doped n- epitaxial layer 24, and a gate electrode 28. Gate electrode 28 comprises a conductive polysilicon that fills a trench 14. A gate oxide 26 coats the walls of the trench and underlies the polysilicon. The top surface of the polysilicon is recessed from the surface 30 of the semiconductor substrate by a distance R (typically from about 0 to $0.4\text{ }\mu\text{m}$). N+ doped source regions 32a, 32b are positioned one on each side of the trench 14. A dielectric layer 35 covers the trench opening and the two source regions 32a, 32b. Extending between the source regions of adjacent cells is a p+ heavy body region 34 and, beneath it,

US 6,521,497 B2

5

a flat-bottomed p- well **36**. In the areas of the cell array which have a n+ contact **16**, a shallow n+ doped contact region extends between the n+source regions. A source metal layer **38** covers the surface of the cell array.

The transistor shown in FIGS. **1a** and **1b** includes several features that enhance the ruggedness of the transistor and its resistance to avalanche breakdown degradation.

First, the depth of the p+ heavy body region **34** relative to the depths of the trench **14** and the flat bottom of the p- well is selected so that the peak electric field when voltage is applied to the transistor will be approximately halfway between adjacent trenches. The preferred relative depths of the p+heavy body, the p- well and the trench are different for different device layouts. However, preferred relative depths can be readily determined empirically (by observing the location of peak electric field) or by finite element analysis.

Second, the bottom corners of the trench **14** are rounded (preferably, the top corners are also rounded; this feature is not shown). Corner rounding can be achieved using the process described in copending application U.S. Ser. No. 08/959,197, filed on Oct. 28, 1997. The rounded corners of the trench also tend to cause the peak electric field to be moved away from the trench corners and towards a central location between adjacent trenches.

Third, an abrupt junction at the interface between the p+ heavy body and the p- well causes the peak electric field to occur in that area of the interface. Avalanche multiplication initiates at the location of the peak electric field, thus steering hot carriers away from the sensitive gate oxide and channel regions. As a result, this structure improves reliability and avalanche ruggedness without sacrificing cell density as much as a deeper heavy body junction. This abrupt junction can be achieved by the double doping process that will be described below, or by other processes for forming abrupt junctions, many of which are known in the semiconductor field.

Lastly, referring to FIG. **2**, the cell array is surrounded by a field termination junction **40** which increases the breakdown voltage of the device and thaws avalanche current away from the cell array to the periphery of the die. Field termination junction **40** is a deep p+ well, preferably from about 1 to 3 μm deep at its deepest point, that is deeper than the p+ heavy body regions **34** in order to reduce the electric field caused by the junction curvature. A preferred process for making the above-described transistors is shown as a flow diagram in FIG. **3**, and the individual steps are shown schematically in FIGS. **4-4k**. It is noted that some steps that are conventional or do not require illustration are described below but not shown in FIGS. **4-4k**. As indicated by the arrows in FIG. **3**, and as will be discussed below, the order of the steps shown in FIGS. **4-4k** can be varied. Moreover, some of the steps shown in FIGS. **4-4k** are optional, as will be discussed.

A semiconductor substrate is initially provided. Preferably, the substrate is a N++ Si substrate, having a standard thickness, e.g., 500 μm , and a very low resistivity, e.g., 0.001 to 0.005 Ohm-cm. An epitaxial layer is deposited onto this substrate, as is well known, preferably to a thickness of from about 4 to 10 μm . Preferably the resistivity of the epitaxial layer is from about 0.1 to 3.0 Ohm-cm.

Next, the field termination junction **40** is formed by the steps shown in FIGS. **4-4c**. FIG. **4**, an oxide layer is formed on the surface of the epitaxial layer. Preferably, the thickness of the oxide is from about 5 to 10 kÅ. Next, as shown in FIG. **4a**, the oxide layer is patterned and etched to define a mask, and the p+ dopant is introduced to form the deep p+ well

6

field termination. A suitable dopant is boron, implanted at an energy of from about 40 to 100 keV and a dose of $1\text{E}14$ (1×10^{14}) to $1\text{E}16$ cm^{-2} . As shown in FIG. **4b**, the p+ dopant is then driven further into the substrate, e.g., by diffusion, and a field oxide layer is formed over the p+ junction. Preferably the oxide thickness is from about 4 to 10 kÅ. Finally, the oxide (FIG. **4**) over the active area of the substrate (the area where the cell array will be formed) is patterned and removed by any suitable etching process, leaving only the field oxide in suitable areas. This leaves the substrate ready for the following steps that will form the cell array.

It is noted that, as an alternative to steps **4-4c**, a suitable field termination structure can be formed using a ring-shaped trench which surrounds the periphery of the cell array and acts to lessen the electric field and increase the resistance to avalanche breakdown degradation. This trench field termination does not require a field oxide or deep p+ body junction to be effective. Consequently, it can be used to reduce the number of process steps. Using a trench ring (or multiple concentric trench rings) to form a field termination is described in, e.g., U.S. Pat. No. 5,430,324, the full disclosure of which is hereby incorporated herein by reference. Preferably, the trench would have substantially the same depth as the trenches in the cell array.

The cell array is formed by the steps shown in FIGS. **4d-4k**. First, a plurality of trenches are patterned and etched into the epitaxial layer of the substrate (FIG. **4d**). Preferably, as noted above, the trenches are formed using the process described in copending application U.S. Pat. No. 08/959, 197, so that the upper and lower corners of each trench will be smoothly rounded. As shown in FIG. **1** and described above, the trenches are patterned to run in only one direction, defined as an open cell structure. After trench formation, a gate oxide layer is formed on the trench walls, as is well known in the semiconductor field. Preferably the gate oxide has a thickness of from about 100 to 800 Å.

Next, as shown in FIG. **4e**, polysilicon is deposited to fill the trench and cover the surface of the substrate, generally to a thickness of from about 1 to 2 μm depending on the trench width (shown by the dotted lines in FIG. **4e**). This layer is then planarized by the nature of its thickness relative to the trench width, typically from about 2 to 5 k Å (indicated by solid lines in FIG. **4e**). The polysilicon is then doped to n-type, e.g., by conventional POCl_3 doping or by phosphorus implant. The backside of the wafer need not be stripped (as is conventionally done prior to doping the polysilicon to enhance defect gettering) because any further doping of the highly doped substrate would be unlikely to result in any enhancement in defect gettering.

The polysilicon is then patterned with a photoresist mask and etched to remove it from the trench areas, as shown in FIG. **4f**. A small recess between the top of the polysilicon in the trench and the substrate surface inherently results when the polysilicon is etched completely to remove all of the polysilicon from the substrate surface. The depth of this recess must be controlled so that it does not exceed the depth of the n+ source junction that will be formed in a later step. To reduce the need to carefully control this aspect of the process, a relatively deep n+ source junction is formed, as will be discussed below.

Then, as shown in FIG. **4g**, the p- well is formed by implanting the dopant, e.g., a boron implant at an energy of 30 to 100 keV and a dosage of $1\text{E}13$ to $1\text{E}15$, and driving it in to a depth of from about 1 to 3 μm using conventional drive in techniques.

US 6,521,497 B2

7

The next two steps (p+ heavy body formation) can be performed either before formation of the n+ source junction, or afterwards, as indicated by the arrows in FIG. 3. P+ heavy body formation and n+ source junction formation can be performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. 4h. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. 4k, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p- well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$, and a second boron implant at an energy of 20 to 40 keV and a dose of $1\text{E}14$ to $1\text{E}15\text{ cm}^{-2}$. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact 18. The resulting p+ heavy body junction is preferably about 0.4 to 1 μm deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5 μm deep), and includes a region of high dopant concentration near the interface with the p-well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. 5.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts 18 (FIGS. 1 and 1b), as shown in FIG. 4i. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. 4l, which correspond to FIGS. 1a and 1b).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of $5\text{E}15$ to $1\text{E}16\text{ cm}^{-2}$ followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$. The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8 μm after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts 16 (see FIGS. 1 and 1a) by compensating (converting) the p-type

8

surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. 5a and 5b, respectively.

Thus, the alternating p+ and n+ contacts 18, 16, shown in FIG. 1 are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower $R_{ds,on}$.

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900° C., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. 4j), after which the dielectric is patterned and etched (FIG. 4k) to define electrical contact openings over the n+ and p+ contacts 16, 18.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well known in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "if" doped instead, and vice versa.

What is claimed is:

1. A method of making a heavy body structure for a trench DMOS transistor comprising:

providing a semiconductor substrate;

forming a plurality of trenches into the substrate;

implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;

implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body; and

implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body,

wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration that is greater than said dosage of said third dopant.

2. The method of claim 1 wherein said first and second dopants both comprise boron.

3. The method of claim 1 wherein said first energy is from about 30 to 100 keV.

4. The method of claim 3 wherein said first dosage is from about $1\text{E}13$ to $1\text{E}15\text{ cm}^{-2}$.

5. The method of claim 1 wherein said second energy is from about 150 to 200 keV.

US 6,521,497 B2

9

6. The method of claim 5 wherein said second dosage is from about $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$.

7. A method of manufacturing a trench field effect transistor comprising:

forming an epitaxial layer on a semiconductor substrate; 5
patterning and etching a plurality of trenches into the epitaxial layer;

lining each trench with a gate dielectric layer;

depositing polysilicon to fill the dielectric-lined trenches; 10

doping the polysilicon with a dopant of a first type;

patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches; 15

patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells; 20

patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and

applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas, 25

wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively. 30

8. The method of manufacturing a trench field effect transistor of claim 7 wherein the trenches are patterned to extend in one direction and be substantially parallel to each other. 35

9. The method of manufacturing a trench field effect transistor of claim 7 wherein the patterning and implanting steps further comprise arranging the first dopant type contact

10

areas and second dopant type contact areas in alternation and extend linearly between adjacent trenches.

10. The method of manufacturing a trench field effect transistor of claim 7 wherein the implanting step for forming the source regions comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, the second energy and dosage being less than the first energy and dosage, respectively.

11. The method of manufacturing a trench field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.

12. The method of manufacturing a trench field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies. 15

13. The method of manufacturing a trench field effect transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.

14. The method of manufacturing a trench field effect transistor of claim 13 wherein said field termination structure is formed by forming a deep well doped with a dopant of the second dopant type. 20

15. The method of manufacturing a trench field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts. 25

16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about $1\text{E}14$ to $1\text{E}15\text{ cm}^{-2}$. 30

17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.

18. The method of manufacturing a trench field effect transistor of claim 13 wherein said field terminations structure is formed by forming a trench ring. 35

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,521,497 B2
DATED : February 18, 2003
INVENTOR(S) : Mo

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4,

Line 38, should read:

-- Figs. 5, 5a and 5b are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor. --

Signed and Sealed this

Twenty-fourth Day of February, 2004

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a cursive "Dudas".

JON W. DUDAS

Acting Director of the United States Patent and Trademark Office

EXHIBIT D

(12) **United States Patent**
Mo et al.

(10) **Patent No.:** **US 6,828,195 B2**
(45) **Date of Patent:** **Dec. 7, 2004**

(54) **METHOD OF MANUFACTURING A TRENCH TRANSISTOR HAVING A HEAVY BODY REGION**

(75) Inventors: **Brian Sze-Ki Mo**, Fremont, CA (US); **Duc Chau**, San Jose, CA (US); **Steven Sapp**, Felton, CA (US); **Izak Bencuya**, Saratoga, CA (US); **Dean Edward Probst**, West Jordan, UT (US)

(73) Assignee: **Fairchild Semiconductor Corporation**, South Portland, ME (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/347,254**

(22) Filed: **Jan. 17, 2003**

(65) **Prior Publication Data**

US 2003/0127688 A1 Jul. 10, 2003

Related U.S. Application Data

(60) Continuation of application No. 09/854,102, filed on May 9, 2001, now Pat. No. 6,521,497, which is a division of application No. 08/970,221, filed on Nov. 14, 1997, now Pat. No. 6,429,481.

(51) **Int. Cl.**⁷ **H01L 21/336**

(52) **U.S. Cl.** **438/270; 438/589**

(58) **Field of Search** **438/270-272, 438/589**

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,070,690 A 1/1978 Wickstrom
4,132,998 A 1/1979 Dingwall
4,145,703 A 3/1979 Blanchard et al.
4,326,332 A 4/1982 Kenney
4,329,705 A 5/1982 Baker
4,344,081 A 8/1982 Pao et al.
4,345,265 A 8/1982 Blanchard

4,398,339 A 8/1983 Blanchard et al.
4,503,449 A 3/1985 David et al.
4,503,598 A 3/1985 Vora et al.
4,541,001 A 9/1985 Schutten et al.
4,639,762 A 1/1987 Neilson et al.
4,682,405 A 7/1987 Blanchard et al.
4,683,643 A 8/1987 Nakajima et al.

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

CN 1090680 A 4/1994
EP 56131960 A 10/1981
EP 0 238 749 A2 9/1987
EP 0 550 770 B1 7/1993
EP 0 583 028 A1 2/1994

(List continued on next page.)

OTHER PUBLICATIONS

Blanchard, R.A., "Optimization of discrete high power MOS transistors," *Stanford Electronics Laboratory, Integrated Circuits Laboratory*, Apr. 1982, Technical Report No. IDEZ696-2.

Chang, T.S. and Critchlow, D.L., "Verticle FET random-access memories with deep trench isolation," *IBM Technical Disclosure Bulletin*, Jan. 1980, pp. 3683-3687, vol. 22(8B).

(List continued on next page.)

Primary Examiner—John F. Niebling

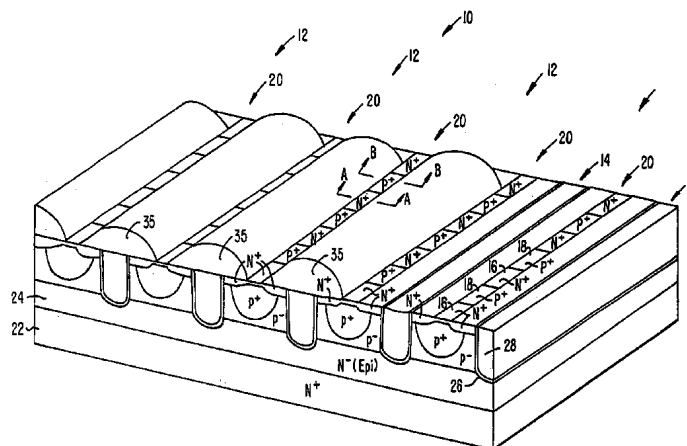
Assistant Examiner—Angel Roman

(74) *Attorney, Agent, or Firm*—Babak S. Sani; Townsend and Townsend and Crew LLP

(57) **ABSTRACT**

A trenched field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

23 Claims, 9 Drawing Sheets



US 6,828,195 B2

Page 2

U.S. PATENT DOCUMENTS

4,767,722 A	8/1988	Blanchard	
4,808,543 A	2/1989	Parrillo et al.	
4,845,537 A	7/1989	Nishimura et al.	
4,860,072 A	8/1989	Zommer	
4,881,105 A	11/1989	Davari et al.	
4,893,160 A	1/1990	Blanchard	
4,914,058 A	4/1990	Blanchard	
4,967,245 A	10/1990	Cogan et al.	
4,983,535 A	1/1991	Blanchard	
5,016,068 A	5/1991	Mori	
5,017,504 A	5/1991	Nishimura et al.	
5,045,900 A	9/1991	Tamagawa	
5,072,266 A	12/1991	Bulucea et al.	
5,124,764 A	6/1992	Mori	
5,160,491 A	11/1992	Mori	
5,168,331 A	12/1992	Yilmaz	
5,298,442 A	3/1994	Bulucea et al.	
5,298,780 A	3/1994	Harada	
5,316,959 A	5/1994	Kwan et al.	
5,321,289 A	6/1994	Baba et al.	
5,341,011 A	8/1994	Hshieh et al.	
5,405,794 A	4/1995	Kim	
5,410,170 A	4/1995	Bulucea et al.	
5,430,324 A	7/1995	Bencuya	
5,455,190 A	10/1995	Hsu	
5,460,985 A	10/1995	Tokura et al.	
5,468,982 A	11/1995	Hshieh et al.	
5,474,943 A	12/1995	Hshieh et al.	
5,508,534 A	4/1996	Nakamura et al.	
5,532,179 A	7/1996	Chang et al.	
5,541,425 A	7/1996	Nishihara	
5,558,313 A	9/1996	Hshieh et al.	
5,567,634 A	10/1996	Hebert et al.	
5,578,851 A	11/1996	Hshieh et al.	
5,592,005 A	1/1997	Floyd et al.	
5,597,765 A	1/1997	Yilmaz et al.	
5,602,046 A	2/1997	Calafut et al.	
5,605,852 A	2/1997	Bencuya	
5,614,751 A	3/1997	Yilmaz et al.	
5,629,543 A	5/1997	Hshieh et al.	
5,639,676 A	6/1997	Hshieh et al.	
5,648,670 A	7/1997	Blanchard	
5,661,322 A	8/1997	Williams et al.	
5,665,619 A	9/1997	Kwan et al.	
5,665,996 A	9/1997	Williams et al.	
5,674,766 A	10/1997	Darwish et al.	
5,679,966 A *	10/1997	Baliga et al.	257/139
5,688,725 A	11/1997	Darwish et al.	
5,689,128 A	11/1997	Hshieh et al.	
5,701,026 A	12/1997	Fujishima et al.	
5,763,915 A	6/1998	Hshieh et al.	
5,767,550 A	6/1998	Calafut et al.	
5,776,812 A	7/1998	Takahashi et al.	
5,780,324 A	7/1998	Tokura et al.	
5,783,491 A	7/1998	Nakamura et al.	
5,801,408 A	9/1998	Takahashi	
5,814,858 A *	9/1998	Williams	257/328
5,879,971 A	3/1999	Witek	
5,895,952 A	4/1999	Darwish et al.	
5,930,630 A	7/1999	Hshieh et al.	
5,986,304 A *	11/1999	Hshieh et al.	257/330
5,998,836 A	12/1999	Williams	
5,998,837 A	12/1999	Williams	
6,015,737 A	1/2000	Tokura et al.	
6,049,108 A	4/2000	Williams et al.	
6,121,089 A *	9/2000	Zeng et al.	438/268
6,204,533 B1	3/2001	Williams et al.	
2002/0185679 A1 *	12/2002	Baliga	257/329

FOREIGN PATENT DOCUMENTS

EP	0 698 919 A2	2/1996
EP	0 720 235 A2	7/1996
EP	0 720 236 A2	7/1996
EP	0 746 030 A2	12/1996
EP	0 755 076 A2	1/1997
EP	0 795 911 A2	9/1997
EP	0 801 425 A1	10/1997
GB	2269050 A	1/1994
JP	57018365 A	1/1982
JP	57153469 A	9/1982
JP	58137254 A	8/1983
JP	58210678 A	12/1983
JP	59080970 A	5/1984
JP	5919064 A	11/1984
JP	60028271 A	2/1985
JP	61102782 A	5/1986
JP	62012167 A	1/1987
JP	62016572 A	1/1987
JP	62023171 A	1/1987
JP	62046569 A	2/1987
JP	63114173 A	5/1988
JP	05226661 A	9/1993
JP	08204194 A	8/1996
JP	08250731 A	9/1996
JP	08316479 A	11/1996
JP	09036362 A	2/1997
JP	09102607 A	4/1997
JP	09270512 A	10/1997
WO	WO 93/03502 A1	2/1993
WO	WO 95/34094 A1	12/1995
WO	WO 97/16853 A1	5/1997
WO	WO 97/07547 A1	12/1997

OTHER PUBLICATIONS

Grant, D.A. and Gower, J., "The development of power MOS devices," Chapter 1.2 In *Power Mosfets: Theory and applications*. John Wiley & Sons; New York, 1989, pp. 5-23.

Goodenough, F., "Dense MOSFET enables portable power control," *Electronic Design* Apr. 14, 1997, pp. 45-50.

Holmes, F.E., and Salama, C.A.T., "V groove M.O.S. transistor technology," *Electronic Letters*, Sep. 20, 1973, pp. 457-458, vol. 9(19).

Holmes, F.E., and Salama, C.A.T., "VMOS-A new MOS integrated circuit technology," *Solid State Electronics* 1974, pp. 791-797, vol. 17.

Lidow, A. et al., "Power Mosfet technology," *IEEE Technical Digest-Int. Electron Devices Meet.* 1979, pp. 79-83.

Lisiak, K.P. and Berger, J., "Optimization of nonplanar power MOS transistors," *IEEE Transactions on Electron Devices*, Oct. 1978, pp. 1229-1234, vol. Ed-25(10).

Ou-Yang, P., "Double ion implanted V-MOS technology," *IEEE Journal of Solid-State Circuits*, Feb. 1977, pp. 3-10, vol. SC-12(1)

Salama, C.A. and Oakes, J.G., "Nonplanar power field-effect transistors," *IEEE Transactions on Electron Devices*, Oct. 1978, pp. 1222-1228, vol. Ed-25(10).

Sun, S.C., "Physics and technology of power MOSFETs," *Stanford Electronics Laboratory, Integrated Circuits Laboratory*, Feb. 1982, Technical Report No. IDEZ696-1.

Sze, S.M., "P-N Junction diode," Chapter 2 In *Physics of Semiconductor Devices*. Second Edition, John Wiley & Sons; New York, 1981, pp. 63-108.

* cited by examiner

U.S. Patent

Dec. 7, 2004

Sheet 1 of 9

US 6,828,195 B2

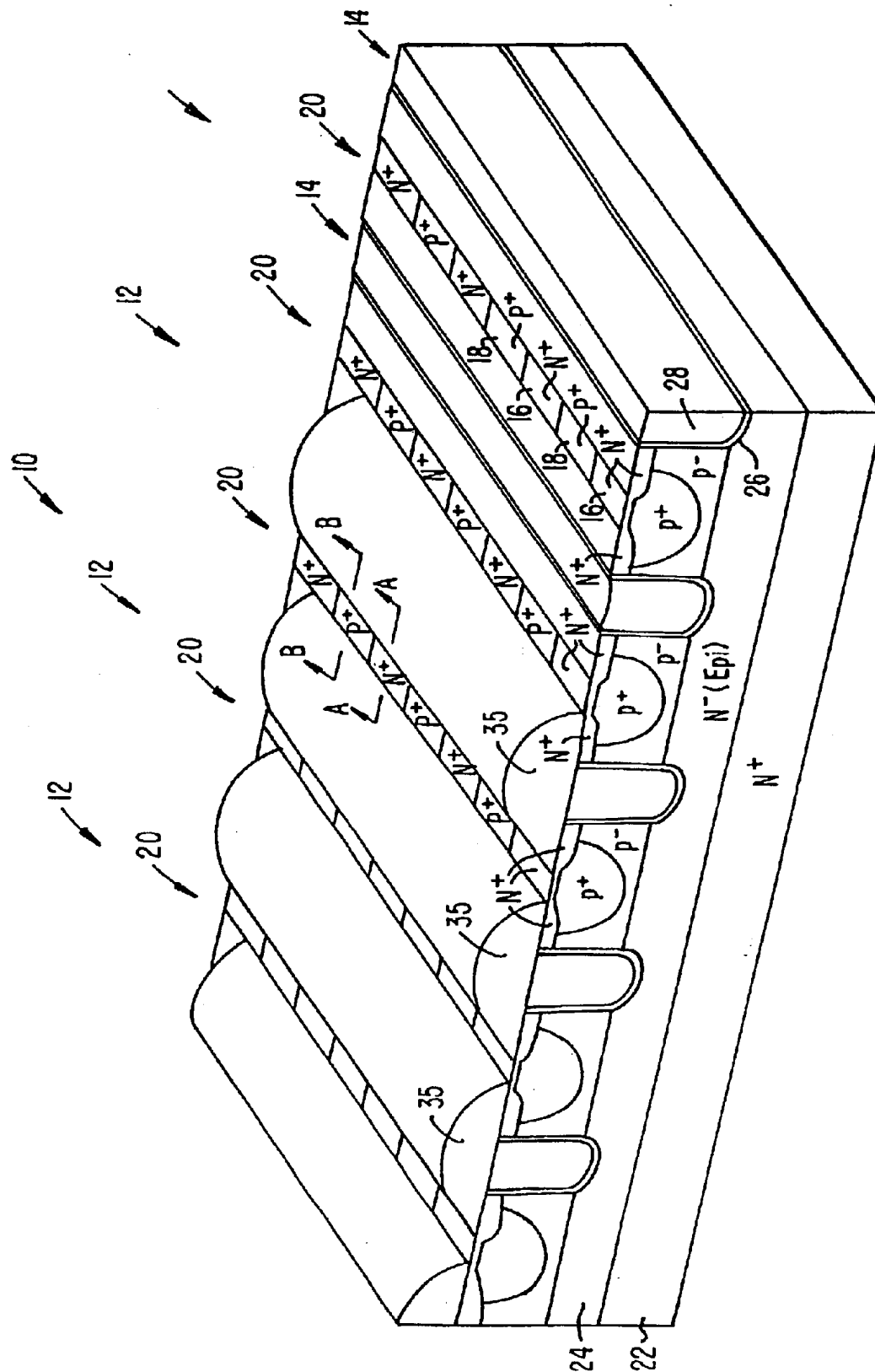


FIG. 1.

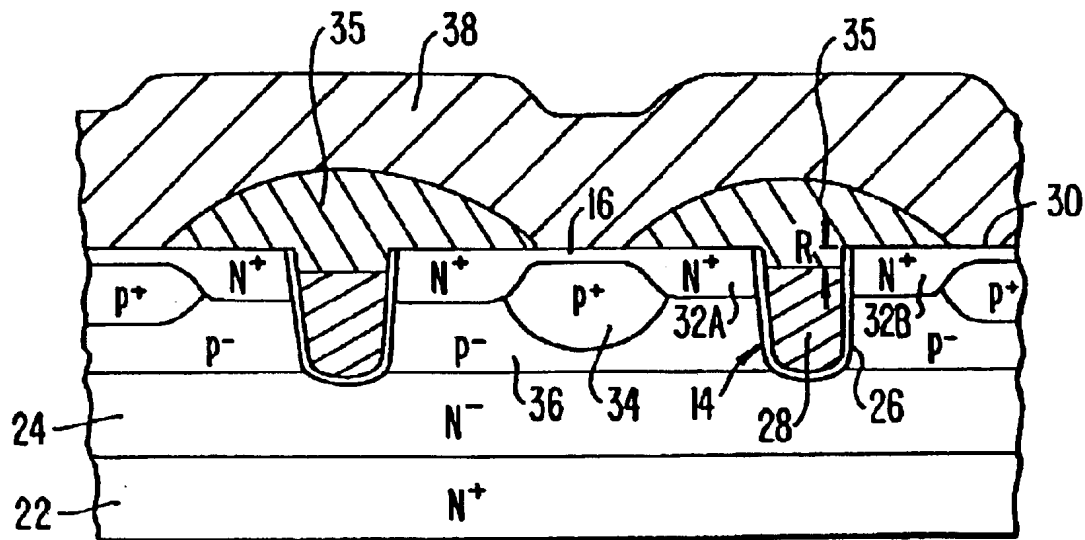


FIG. 1A.

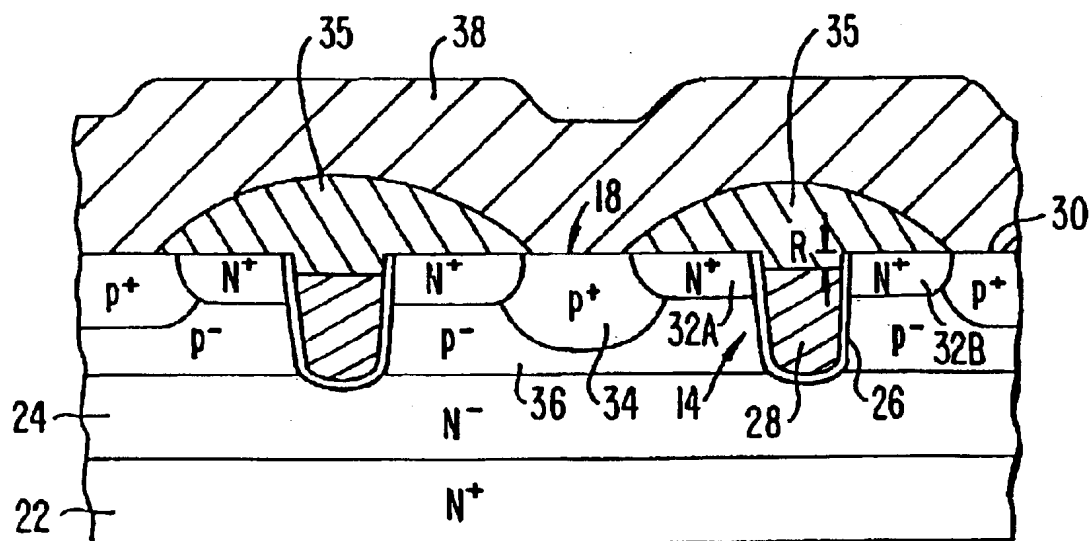


FIG. 1B.

U.S. Patent

Dec. 7, 2004

Sheet 3 of 9

US 6,828,195 B2

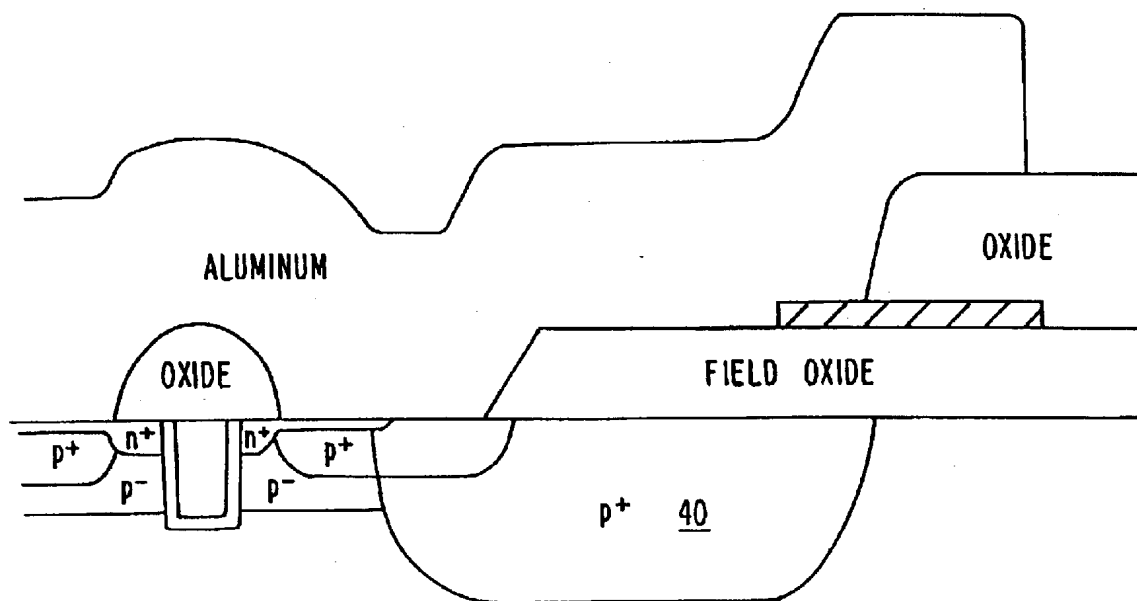


FIG. 2.

U.S. Patent

Dec. 7, 2004

Sheet 4 of 9

US 6,828,195 B2

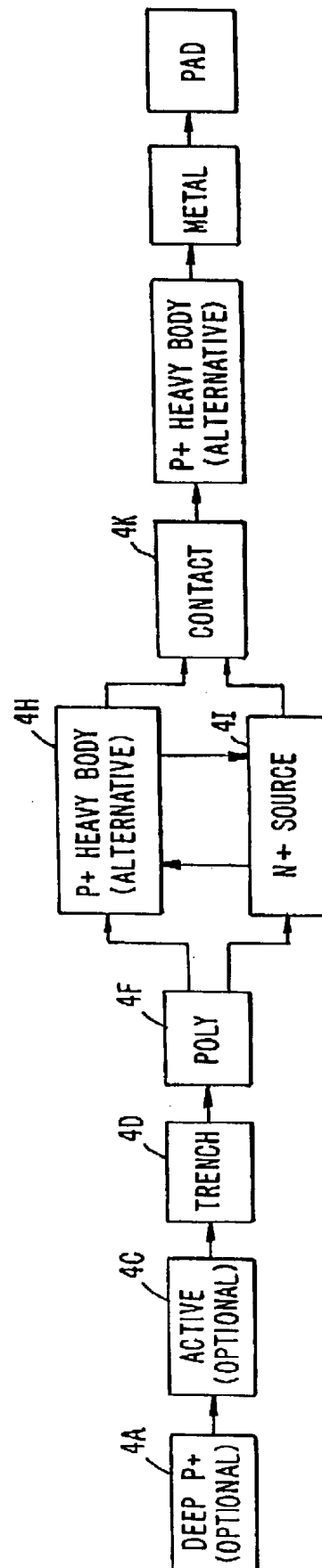


FIG. 3.

U.S. Patent

Dec. 7, 2004

Sheet 5 of 9

US 6,828,195 B2

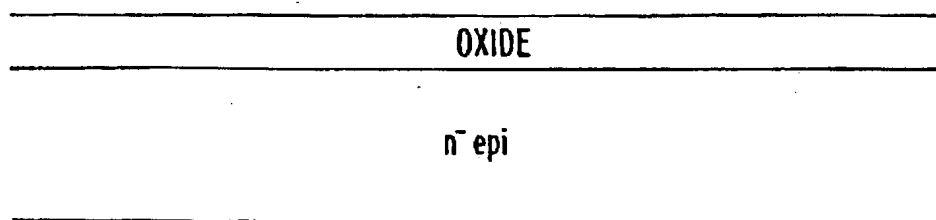


FIG. 4.

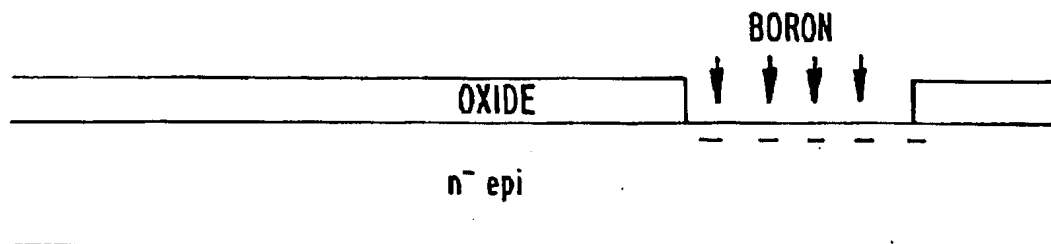


FIG. 4A.

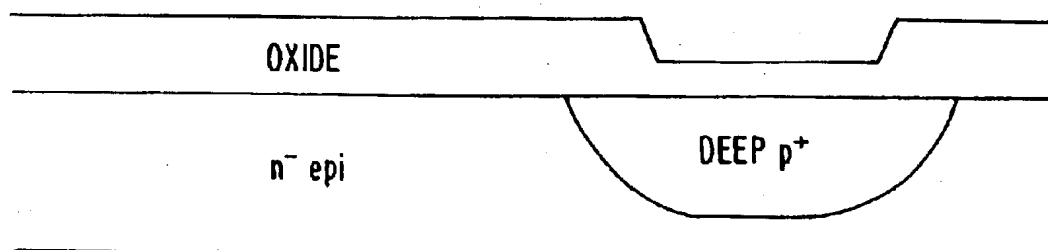


FIG. 4B.

U.S. Patent

Dec. 7, 2004

Sheet 6 of 9

US 6,828,195 B2

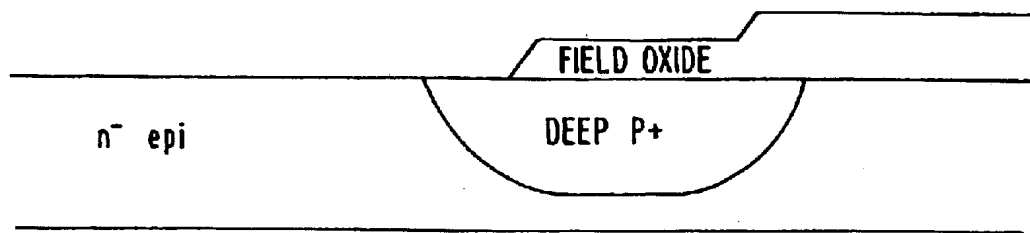


FIG. 4C.

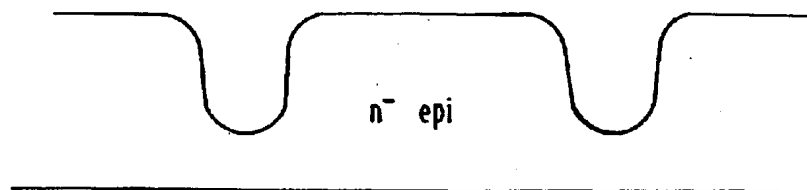


FIG. 4D.

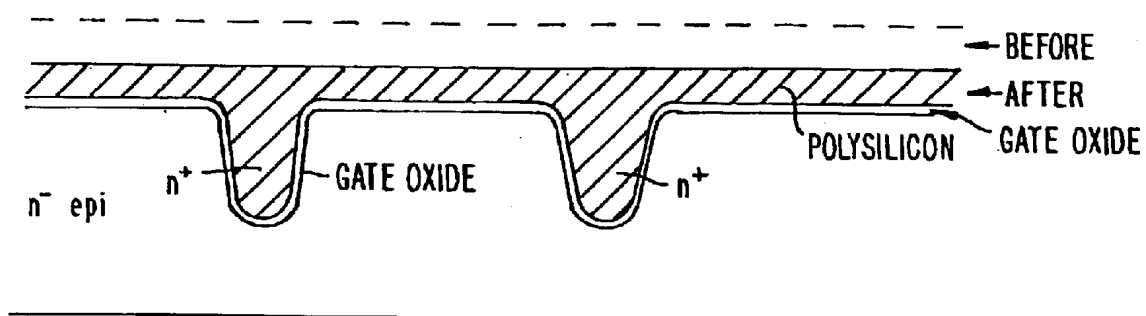


FIG. 4E.

U.S. Patent

Dec. 7, 2004

Sheet 7 of 9

US 6,828,195 B2

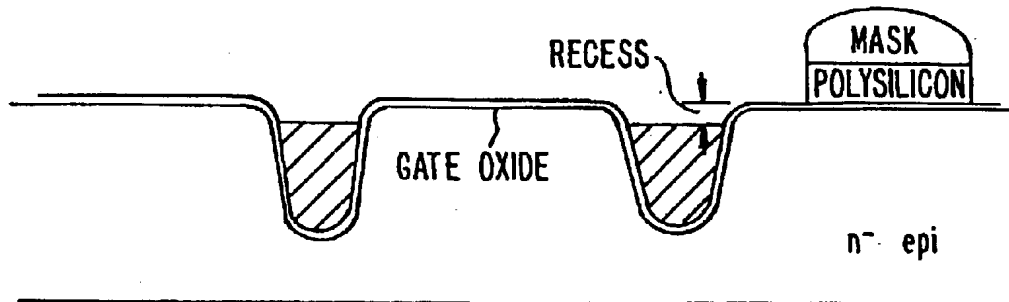


FIG. 4F.

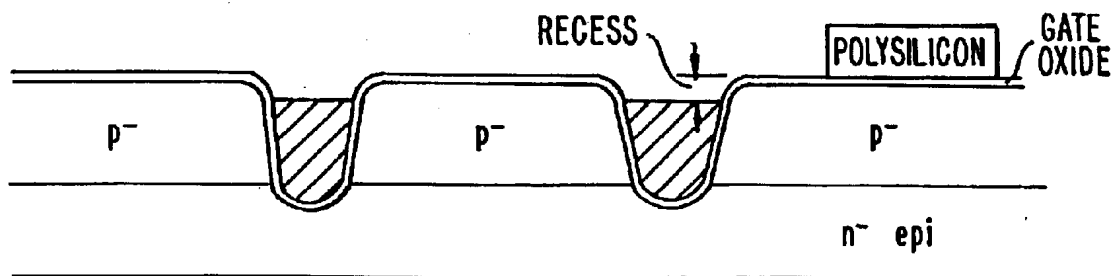


FIG. 4G.

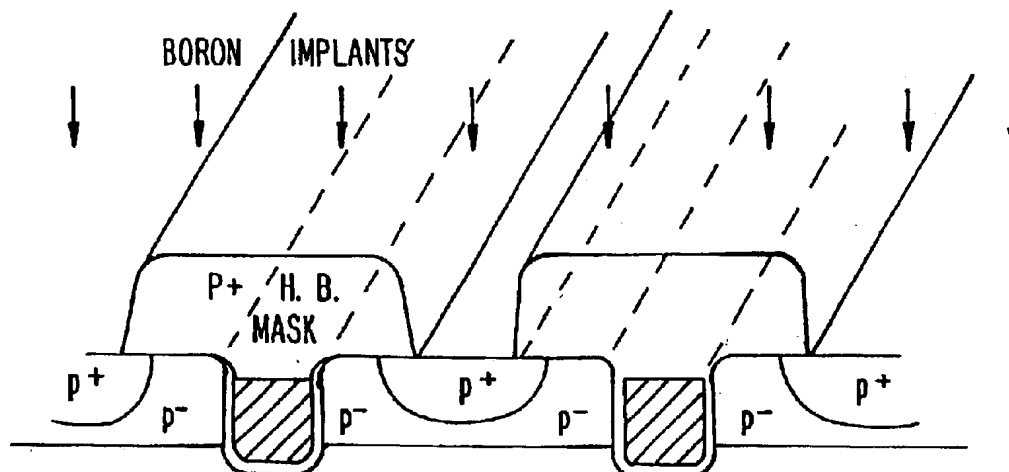


FIG. 4H.

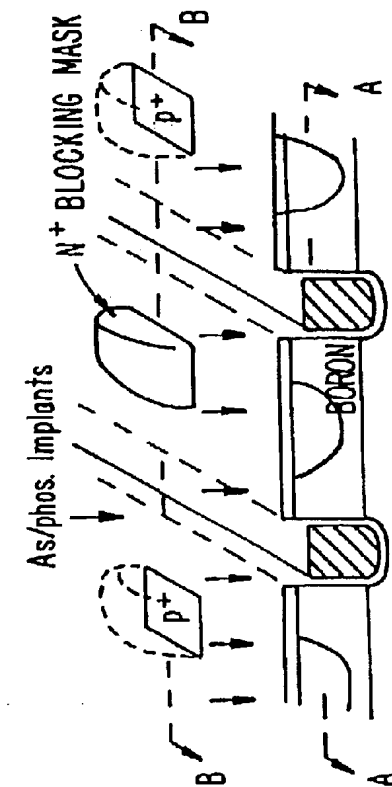


FIG. 4I.

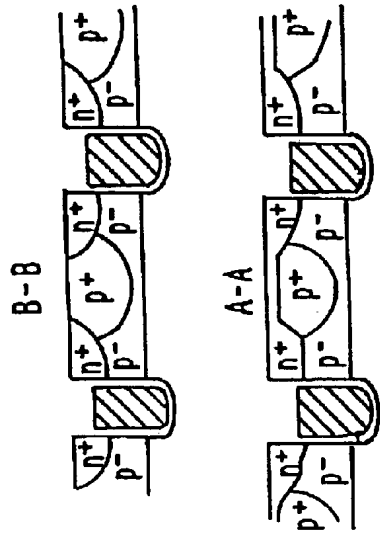


FIG. 4J.

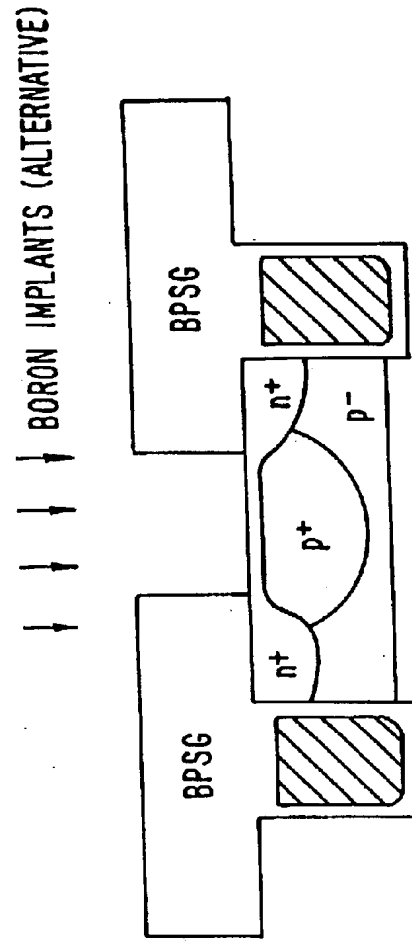


FIG. 4K.

U.S. Patent

Dec. 7, 2004

Sheet 9 of 9

US 6,828,195 B2

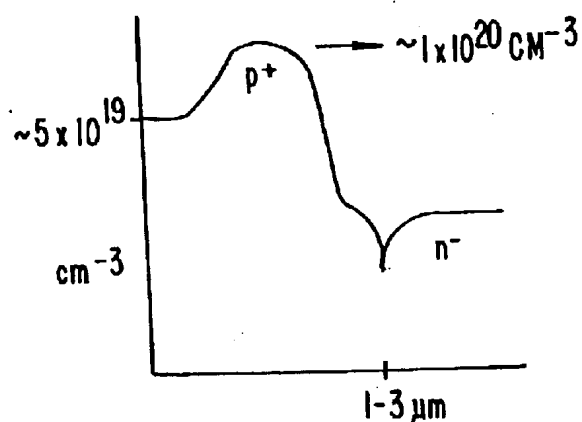


FIG. 5.

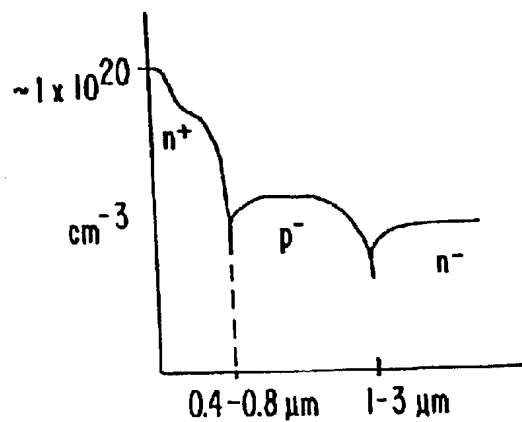


FIG. 5A.

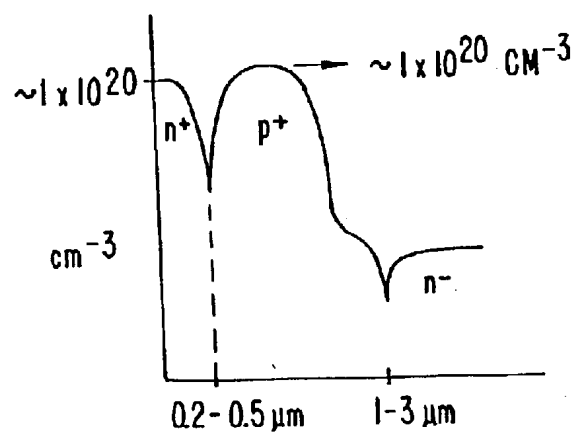


FIG. 5B.

US 6,828,195 B2

1

METHOD OF MANUFACTURING A TRENCH TRANSISTOR HAVING A HEAVY BODY REGION

This application is a continuation of and claims the benefit of U.S. application Ser. No. 09/854,102 filed May 9, 2001, now U.S. Pat. No. 6,521,497, which is a divisional of U.S. application Ser. No. 08/970,221 filed Nov. 14, 1997.

BACKGROUND OF THE INVENTION

The present invention relates to field effect transistors, in particular trench DMOS transistors, and methods of their manufacture.

Power field effect transistors, e.g., MOSFETs (metal oxide semiconductor field effect transistors), are well known in the semiconductor industry. One type of MOSFET is a DMOS (double diffused metal oxide semiconductor) transistor. DMOS transistors typically include a substrate on which an epitaxial layer is grown, a doped source junction, a doped heavy body, a doped well of the same (p or n) doping as the heavy body, and a gate electrode. In trenched DMOS transistors the gate electrode is a vertical trench. The heavy body is typically diffused deeper than the bottom of the trench, to minimize electric field at the bottom corners of the trench and thereby prevent avalanche breakdown from damaging the device. The trench is filled with conductive polysilicon, and the polysilicon is generally overetched, to assure that it is completely removed from the surface surrounding the trench. This overetching generally leaves a recess between the top of the polysilicon and the surface of the semiconductor substrate (i.e., the surface of the epitaxial layer). The depth of this recess must be carefully controlled so that it is shallower than the depth of the source junctions. If the recess is deeper than the source junctions the source may miss the gate, resulting in high on-state resistance, high threshold, and potentially a non-functional transistor.

The source and drain junctions can be doped with either p-type or n-type dopants; in either case, the body will be doped with the opposite dopant, e.g., for n-type source and drain the body will be p-type. DMOS transistors in which the source and drain are doped with p-type carriers are referred to as "p-channel". In p-channel DMOS transistors a negative voltage applied to the transistor gate causes current flow from the source region, through a channel region of the body, an accumulation region of the epitaxial layer, and the substrate, to the drain region. Conversely, DMOS transistors, in which the source and drain are doped with n-type carriers, are referred to as "n-channel". In n-channel DMOS transistors a positive voltage applied to the transistor gate causes current to flow from drain to source.

It is desirable that DMOS transistors have low source to drain resistance ($R_{ds_{on}}$) when turned on and low parasitic capacitance. The transistor structure should also avoid "punchthrough". Punchthrough occurs when, upon application of a high drain to source voltage, depletion into the body region extends to the source region, forming an undesirable conductive path through the body region when the transistor should be off. Finally, the transistor should have good "ruggedness", i.e., a high activation current is needed to turn on the parasitic transistor that inherently exists in DMOS transistors.

Generally a large number of MOSFET cells are connected in parallel forming a single transistor. The cells may be arranged in a "closed cell" configuration, in which the trenches are laid out in a grid pattern and the cells are enclosed on all sides by trench walls. Alternatively, the cells

2

may be arranged in an "open cell" configuration, in which the trenches are laid out in a "stripe" pattern and the cells are only enclosed on two sides by trench walls. Electric field termination techniques are used to terminate junctions (doped regions) at the periphery (edges) of the silicon die on which the transistors are formed. This tends to cause the breakdown voltage to be higher than it would otherwise be if controlled only by the features of the active transistor cells in the central portions of the die.

SUMMARY OF THE INVENTION

The present invention provides field effect transistors that have an open cell layout that provides good uniformity and high cell density and that is readily scalable. Preferred trenched DMOS transistors exhibit low $R_{ds_{on}}$, low parasitic capacitance, excellent reliability, resistance to avalanche breakdown degradation, and ruggedness. Preferred devices also include a field termination that enhances resistance to avalanche breakdown. The invention also features a method of making trench DMOS transistors.

In one aspect, the invention features a trenched field effect transistor that includes

(a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of the heavy body region relative to the depths of the well and the trench is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped well has a depth less than the predetermined depth of the trench. The trench has rounded top and bottom corners. There is an abrupt junction at the interface between the heavy body and the well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface.

In another aspect, the invention features an array of transistor cells. The array includes (a) a semiconductor substrate, (b) a plurality of gate-forming trenches arranged substantially parallel to each other and extending in a first direction, the space between adjacent trenches defining a contact area, each trench extending a predetermined depth into said substrate, the predetermined depth being substantially the same for all of said gate-forming trenches; (c) surrounding each trench, a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, (d) positioned between each pair of gate-forming trenches, a doped heavy body positioned adjacent each source junction, the deepest portion of each said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches, (e) a doped well surrounding each heavy body beneath the heavy body; and (f) p+ and n+ contacts disposed at the surface of the semiconductor substrate and arranged in alternation along the length of the contact area.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about $1E15$ to $5E15$ cm^{-2} . The second energy is from about 20 to 40 keV. The second dosage is from about $1E14$ to $1E15$ cm^{-2} .

US 6,828,195 B2

3

In yet another aspect, the invention features a semiconductor die that includes (a) a plurality of DMOS transistor cells arranged in an array on a semiconductor substrate, each DMOS transistor cell including a gate-forming trench, each of said gate-forming trenches having a predetermined depth, the depth of all of the gate-forming trenches being substantially the same; and (b) surrounding the periphery of the array, a field termination structure that extends into the semiconductor substrate to a depth that is deeper than said predetermined depth of said gate-forming trenches.

Preferred embodiments include one or more of the following features. The first dopant comprises arsenic and the second dopant comprises phosphorus. The first energy is from about 80 to 120 keV. The first dosage is from about 5×10^{15} to $1 \times 10^{16} \text{ cm}^{-2}$. The second energy is from about 40 to 70 keV. The second dosage is from about 1×10^{15} to $5 \times 10^{15} \text{ cm}^{-2}$. The resulting depth of the source is from about 0.4 to $0.8 \mu\text{m}$ the finished DMOS transistor.

The invention also features a method of making a heavy body structure for a trench DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into said region a second dopant at a second energy and dosage, said second energy and dosage being relatively less than said first energy and dosage.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about 1×10^{15} to 5×10^{15} . The second energy is from about 20 to 40 keV. The second dosage is from about 1×10^{14} to 1×10^{15} .

Additionally, the invention features a method of making a source for a trench DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into the region a second dopant at a second energy and dosage, the second energy and dosage being relatively less than the first energy and dosage.

Preferred embodiments include one or more of the following features. The first dopant comprises arsenic and the second dopant comprises phosphorus. The first energy is from about 80 to 120 keV. The first dosage is from about 5×10^{15} to 1×10^{16} . The second energy is from about 40 to 70 keV. The second dosage is from about 1×10^{15} to 5×10^{15} . The resulting depth of the source is from about 0.4 to $0.8 \mu\text{m}$ in the finished DMOS transistor.

In another aspect, the invention features a method of manufacturing a trench field effect transistor. The method includes (a) forming a field termination junction around the perimeter of a semiconductor substrate, (b) forming an epitaxial layer on the semiconductor substrate, (c) patterning and etching a plurality of trenches into the epitaxial layer; (d) depositing polysilicon to fill the trenches, (e) doping the polysilicon with a dopant of a first type, (f) patterning the substrate and implanting a dopant of a second, opposite type to form a plurality of wells interposed between adjacent trenches, (g)

patterning the substrate and implanting a dopant of the second type to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned above the wells, each heavy body having an abrupt junction with the corresponding well, (h) patterning the substrate and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and (i) applying a dielectric to the surface of the

4

semiconductor substrate and patterning the dielectric to expose electrical contact areas.

Other features and advantages of the invention will be apparent from the following detailed description, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a highly enlarged, schematic perspective cross-sectional view showing a portion of a cell array including a plurality of DMOS transistors according to one aspect of the invention. The source metal layer and a portion of the dielectric layer have been omitted to show the underlying layers. FIGS. 1a and 1b are side cross-sectional views of a single line of transistors from the array of FIG. 1, taken along lines A—A and B—B, respectively. In FIGS. 1a and 1b the source metal and dielectric layers are shown.

FIG. 2 is a highly enlarged schematic side cross-sectional view of a semiconductor die showing a portion of the cell array and the field termination.

FIG. 3 is a flow diagram showing the photo mask sequence of a preferred process for forming a trench DMOS transistor of FIG. 1.

FIGS. 4–4k are schematic side cross-sectional views showing the individual steps of the process diagrammed in FIG. 3. The figure numbers for the detailed views in FIGS. 4–4k are shown parenthetically under the corresponding diagram boxes in FIG. 3.

FIGS. 5–5b are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A cell array 10, including a plurality of rows 12 of trench DMOS transistors, is shown in FIG. 1. Cell array 10 has an open cell configuration, i.e., trenches 14 run in only one direction, rather than forming a grid. Individual cells are formed by alternating n+ source contacts 16 and p+ contacts 18 in rows 20 that run parallel to and between trenches 14. The configuration of the regions of each row that have an n+ source contact are shown in cross-section in FIG. 1a, while the regions that have a p+ contact are shown in FIG. 1b.

As shown in FIGS. 1a and 1b, each trench DMOS transistor includes a doped n+ substrate (drain) layer 22, a more lightly doped n- epitaxial layer 24, and a gate electrode 28. Gate electrode 28 comprises a conductive polysilicon that fills a trench 14. A gate oxide 26 coats the walls of the trench and underlies the polysilicon. The top surface of the polysilicon is recessed from the surface 30 of the semiconductor substrate by a distance R (typically from about 0 to $0.4 \mu\text{m}$). N+ doped source regions 32a, 32b are positioned one on each side of the trench 14. A dielectric layer 35 covers the trench opening and the two source regions 32a, 32b. Extending between the source regions of adjacent cells is a p+ heavy body region 34 and, beneath it, a flat-bottomed p- well 36. In the areas of the cell array which have a n+ contact 16, a shallow n+ doped contact region extends between the n+ source regions. A source metal layer 38 covers the surface of the cell array.

The transistor shown in FIGS. 1a and 1b includes several features that enhance the ruggedness of the transistor and its resistance to avalanche breakdown degradation.

First, the depth of the p+ heavy body region 34 relative to the depths of the trench 14 and the flat bottom of the p- well

US 6,828,195 B2

5

is selected so that the peak electric field when voltage is applied to the transistor will be approximately halfway between adjacent trenches. The preferred relative depths of the p+ heavy body, the p- well and the trench are different for different device layouts. However, preferred relative depths can be readily determined empirically (by observing the location of peak electric field) or by finite element analysis.

Second, the bottom corners of the trench **14** are rounded (preferably, the top corners are also rounded; this feature is not shown). Corner rounding can be achieved using the process described in U.S. application Ser. No. 08/959,197, filed on Oct. 28, 1997, now U.S. Pat. No. 6,103,635. The rounded corners of the trench also tend to cause the peak electric field to be moved away from the trench corners and towards a central location between adjacent trenches.

Third, an abrupt junction at the interface between the p+ heavy body and the p- well causes the peak electric field to occur in that area of the interface. Avalanche multiplication initiates at the location of the peak electric field, thus steering hot carriers away from the sensitive gate oxide and channel regions. As a result, this structure improves reliability and avalanche ruggedness without sacrificing cell density as much as a deeper heavy body junction. This abrupt junction can be achieved by the double doping process that will be described below, or by other processes for forming abrupt junctions, many of which are known in the semiconductor field.

Lastly, referring to FIG. **2**, the cell array is surrounded by a field termination junction **40** which increases the breakdown voltage of the device and draws avalanche current away from the cell array to the periphery of the die. Field termination junction **40** is a deep p+ well, preferably from about 1 to 3 μm deep at its deepest point, that is deeper than the p+ heavy body regions **34** in order to reduce the electric field caused by the junction curvature. A preferred process for making the above-described transistors is shown as a flow diagram in FIG. **3**, and the individual steps are shown schematically in FIGS. **4-4k**. It is noted that some steps that are conventional or do not require illustration are described below but not shown in FIGS. **4-4k**. As indicated by the arrows in FIG. **3**, and as will be discussed below, the order of the steps shown in FIGS. **4-4k** can be varied. Moreover, some of the steps shown in FIGS. **4-4k** are optional, as will be discussed.

A semiconductor substrate is initially provided. Preferably, the substrate is a N++ Si substrate, having a standard thickness, e.g., 500 μm , and a very low resistivity, e.g., 0.001 to 0.005 Ohm-cm. An epitaxial layer is deposited onto this substrate, as is well known, preferably to a thickness of from about 4 to 10 μm . Preferably the resistivity of the epitaxial layer is from about 0.1 to 3.0 Ohm-cm.

Next, the field termination junction **40** is formed by the steps shown in FIGS. **4-4c**. In FIG. **4**, an oxide layer is formed on the surface of the epitaxial layer. Preferably, the thickness of the oxide is from about 5 to 10 k \AA . Next, as shown in FIG. **4a**, the oxide layer is patterned and etched to define a mask, and the p+ dopant is introduced to form the deep p+ well field termination. A suitable dopant is boron, implanted at an energy of from about 40 to 100 keV and a dose of $1\text{E}14$ (1×10^{14}) to $1\text{E}16$ cm^{-2} . As shown in FIG. **4b**, the p+ dopant is then driven further into the substrate, e.g., by diffusion, and a field oxide layer is formed over the p+ junction. Preferably the oxide thickness is from about 4 to 10 k \AA . Finally, the oxide (FIG. **4**) over the active area of the substrate (the area where the cell array will be formed) is

6

patterned and removed by any suitable etching process, leaving only the field oxide in suitable areas. This leaves the substrate ready for the following steps that will form the cell array.

It is noted that, as an alternative to steps **4-4c**, a suitable field termination structure can be formed using a ring-shaped trench which surrounds the periphery of the cell array and acts to lessen the electric field and increase the resistance to avalanche breakdown degradation. This trench field termination does not require a field oxide or deep p+ body junction to be effective. Consequently, it can be used to reduce the number of process steps. Using a trench ring (or multiple concentric trench rings) to form a field termination is described in, e.g., U.S. Pat. No. 5,430,324, the full disclosure of which is hereby incorporated herein by reference. Preferably, the trench would have substantially the same depth as the trenches in the cell array.

The cell array is formed by the steps shown in FIGS. **4d-4k**. First, a plurality of trenches are patterned and etched into the epitaxial layer of the substrate (FIG. **4d**). Preferably, as noted above, the trenches are formed using the process U.S. application Ser. No. 08/959,197, filed on Oct. 28, 1997, now U.S. Pat. No. 6,103,635, so that the upper and lower corners of each trench will be smoothly rounded. As shown in FIG. **1** and described above, the trenches are patterned to run in only one direction, defined as an open cell structure. After trench formation, a gate oxide layer is formed on the trench walls, as is well known in the semiconductor field. Preferably the gate oxide has a thickness of from about 100 to 800 \AA .

Next, as shown in FIG. **4e**, polysilicon is deposited to fill the trench and cover the surface of the substrate, generally to a thickness of from about 1 to 2 μm depending on the trench width (shown by the dotted lines in FIG. **4e**). This layer is then planarized by the nature of its thickness relative to the trench width, typically from about 2 to 5 k \AA (indicated by solid lines in FIG. **4e**). The polysilicon is then doped to n-type, e.g., by conventional POCL₃ doping or by phosphorus implant. The backside of the wafer need not be stripped (as is conventionally done prior to doping the polysilicon to enhance defect gettering) because any further doping of the highly doped substrate would be unlikely to result in any enhancement in defect gettering.

The polysilicon is then patterned with a photoresist mask and etched to remove it from the trench areas, as shown in FIG. **4f**. A small recess between the top of the polysilicon in the trench and the substrate surface inherently results when the polysilicon is etched completely to remove all of the polysilicon from the substrate surface. The depth of this recess must be controlled so that it does not exceed the depth of the n+ source junction that will be formed in a later step. To reduce the need to carefully control this aspect of the process, a relatively deep n+ source junction is formed, as will be discussed below.

Then, as shown in FIG. **4g**, the p- well is formed by implanting the dopant, e.g., a boron implant at an energy of 30 to 100 keV and a dosage of $1\text{E}13$ to $1\text{E}15$, and driving it in to a depth of from about 1 to 3 μm using conventional drive in techniques.

The next two steps (p+ heavy body formation) can be performed either before formation of the n+ source junction, or afterwards, as indicated by the arrows in FIG. **3**. P+ heavy body formation and n+ source junction formation can be performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process

US 6,828,195 B2

7

flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. 4h. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. 4k, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p- well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$, and a second boron implant at an energy of 20 to 40 keV and a dose of $1\text{E}14$ to $1\text{E}15\text{ cm}^{-2}$. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact 18. The resulting p+ heavy body junction is preferably about 0.4 to $1\text{ }\mu\text{m}$ deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to $1.5\text{ }\mu\text{m}$ deep), and includes a region of high dopant concentration near the interface with the p-well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. 5.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts 18 (FIGS. 1 and 1b), as shown in FIG. 4i. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. 4l, which correspond to FIGS. 1a and 1b).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of $5\text{E}15$ to $1\text{E}16\text{ cm}^{-2}$ followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$. The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to $0.8\text{ }\mu\text{m}$ after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts 16 (see FIGS. 1 and 1a) by compensating (converting) the p-type surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. 5a and 5b, respectively.

Thus, the alternating p+ and n+ contacts 18, 16, shown in FIG. 1 are formed by patterning the substrate with appro-

8

priate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower Rds_{on} .

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900°C ., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. 4j), after which the dielectric is patterned and etched (FIG. 4k) to define electrical contact openings over the n+ and p+ contacts 16, 18.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well known in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "n" doped instead, and vice versa.

What is claimed is:

1. A method of manufacturing a trench transistor comprising:

providing a semiconductor substrate having dopants of a first conductivity type;

forming a plurality of trenches extending to a first depth into the semiconductor substrate;

lining each of the plurality of trenches with a gate dielectric material;

substantially filling each dielectric-lined trench with conductive material;

forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;

forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the well; and

forming a source region inside the well, the source region having dopants of the first conductivity types.

2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.

3. The method of claim 1 further comprising forming a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fourth depth that is deeper than said first depth of the trench.

US 6,828,195 B2

9

4. The method of claim 3 wherein the step of forming a deep doped region forms a PN junction diode with the substrate that helps improve a breakdown voltage of the transistor.

5. The method of claim 3 wherein the deep doped region forms a termination structure around the periphery of the substrate.

6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.

7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.

8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.

9. The method of claim 8 wherein the double implant process comprises:

a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body; and

a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.

10. The method of claim 9 wherein the first implant occurs at approximately the third depth.

11. The method of claim 9 wherein the first energy level is higher than the second energy level.

12. The method of claim 11 wherein the first dosage is higher than the second dosage.

13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.

14. The method of claim 1 wherein the step of forming the heavy body comprises using a continuous dopant source at the surface of the semiconductor substrate.

15. The method of claim 1 wherein the step of forming a plurality of trenches comprises patterning and etching the plurality of trenches that extend in parallel along a longitudinal axis.

16. The method of claim 15 further comprising forming a contact area on the surface of the substrate between adjacent trenches.

17. The method of claim 16 wherein the step of forming the contact area comprises forming alternating source contact regions and heavy body contact regions.

18. The method of claim 16 wherein the step of forming the contact area comprises forming a ladder-shaped source contact region surrounding heavy body contact regions.

10

19. The method claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises:

forming a source blocking mask on the surface of the semiconductor substrate patterned to cover the heavy body contact regions; and

implanting dopants of the first conductivity type to form the ladder-shaped source contact region.

20. The method of claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises forming a dielectric layer on the surface of the semiconductor substrate patterned to expose the heavy body contact regions.

21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:

etching a plurality of trenches into the semiconductor substrate to a first depth;

lining the plurality of trenches with dielectric layer;

substantially filling the dielectric-lined plurality of trenches with conductive material;

forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;

forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type; and

forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type,

wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.

22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.

23. The method of claim 21 further comprising forming a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fourth depth that is deeper than said first depth of the trench.

* * * * *

EXHIBIT E

(12) **United States Patent**
Mo et al.

(10) **Patent No.:** **US 7,148,111 B2**
(45) **Date of Patent:** ***Dec. 12, 2006**

(54) **METHOD OF MANUFACTURING A TRENCH TRANSISTOR HAVING A HEAVY BODY REGION**

(75) Inventors: **Brian Sze-Ki Mo**, Fremont, CA (US); **Duc Chau**, San Jose, CA (US); **Steven Sapp**, Felton, CA (US); **Izak Bencuya**, Saratoga, CA (US); **Dean E. Probst**, West Jordan, UT (US)

(73) Assignee: **Fairchild Semiconductor Corporation**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/927,788**

(22) Filed: **Aug. 27, 2004**

(65) **Prior Publication Data**

US 2005/0079676 A1 Apr. 14, 2005

Related U.S. Application Data

(60) Continuation of application No. 10/347,254, filed on Jan. 17, 2003, now Pat. No. 6,828,195, which is a continuation of application No. 09/854,102, filed on May 9, 2001, now Pat. No. 6,521,497, which is a division of application No. 08/970,221, filed on Nov. 14, 1997, now Pat. No. 6,429,481.

(51) **Int. Cl.**
H01L 21/336 (2006.01)

(52) **U.S. Cl.** **438/270; 438/272; 438/589**

(58) **Field of Classification Search** **438/270, 438/272, 589**

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,070,690 A	1/1978	Wickstrom
4,132,998 A	1/1979	Dingwall
4,145,703 A	3/1979	Blanchard et al.
4,326,332 A	4/1982	Kenney
4,329,705 A	5/1982	Baker
4,344,081 A	8/1982	Pao et al.
4,345,265 A	8/1982	Blanchard
4,398,339 A	8/1983	Blanchard et al.

(Continued)

FOREIGN PATENT DOCUMENTS

CN 1090680 9/1994

(Continued)

OTHER PUBLICATIONS

Blanchard, Richard A., "Optimization of Discrete High Power MOS Transistors," Stanford Electronics Laboratory, Integrated Circuits Laboratory, Technical Report No. IDEZ696-2 (Apr. 1982).

(Continued)

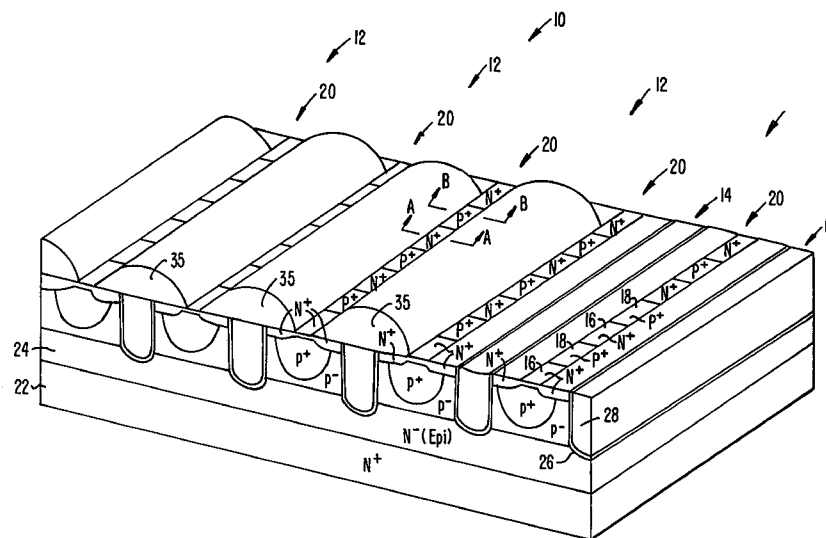
Primary Examiner—Lynne A. Gurley

(74) *Attorney, Agent, or Firm*—Babak S. Sani; Townsend and Townsend and Crew LLP

(57) **ABSTRACT**

A trenched field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

36 Claims, 9 Drawing Sheets



US 7,148,111 B2

Page 2

U.S. PATENT DOCUMENTS

4,503,449 A 3/1985 David et al.
 4,503,598 A 3/1985 Vora et al.
 4,541,001 A 9/1985 Schutten et al.
 4,639,762 A 1/1987 Neilson et al.
 4,682,405 A 7/1987 Blanchard et al.
 4,683,643 A 8/1987 Nakajima et al.
 4,767,722 A 8/1988 Blanchard
 4,808,543 A 2/1989 Parrillo et al.
 4,845,537 A 7/1989 Nishimura et al.
 4,860,072 A 8/1989 Zommer
 4,881,105 A 11/1989 Davari et al.
 4,893,160 A 1/1990 Blanchard
 4,914,058 A 4/1990 Blanchard
 4,967,245 A 10/1990 Cogan et al.
 4,983,535 A 1/1991 Blanchard
 5,016,068 A 5/1991 Mori
 5,017,504 A 5/1991 Nishimura et al.
 5,045,900 A 9/1991 Tamagawa
 5,072,266 A 12/1991 Bulucea et al.
 5,124,764 A 6/1992 Mori
 5,160,491 A 11/1992 Mori
 5,168,331 A 12/1992 Yilmaz
 5,298,442 A 3/1994 Bulucea et al.
 5,298,780 A 3/1994 Harada
 5,316,959 A 5/1994 Kwan et al.
 5,321,289 A 6/1994 Baba et al.
 5,341,011 A 8/1994 Hshieh et al.
 5,405,794 A 4/1995 Kim
 5,410,170 A 4/1995 Bulucea et al.
 5,430,324 A 7/1995 Bencuya
 5,455,190 A 10/1995 Hsu
 5,460,985 A 10/1995 Tokura et al.
 5,468,982 A 11/1995 Hshieh et al.
 5,474,943 A 12/1995 Hshieh et al.
 5,508,534 A 4/1996 Nakamura et al.
 5,532,179 A 7/1996 Chang et al.
 5,541,425 A 7/1996 Nishihara
 5,558,313 A 9/1996 Hshieh et al.
 5,567,634 A 10/1996 Herbert et al.
 5,578,851 A 11/1996 Hshieh et al.
 5,592,005 A 1/1997 Floyd et al.
 5,597,765 A 1/1997 Yilmaz et al.
 5,602,046 A 2/1997 Calafut et al.
 5,605,852 A 2/1997 Bencuya
 5,614,751 A 3/1997 Yilmaz et al.
 5,629,543 A 5/1997 Hshieh et al.
 5,639,676 A 6/1997 Hshieh et al.
 5,648,670 A 7/1997 Blanchard
 5,661,322 A 8/1997 Williams et al.
 5,665,619 A * 9/1997 Kwan et al. 438/270
 5,665,996 A 9/1997 Williams et al.
 5,674,766 A 10/1997 Darwish et al.
 5,679,966 A 10/1997 Baliga et al.
 5,688,725 A 11/1997 Darwish et al.
 5,689,128 A 11/1997 Hshieh et al.
 5,701,026 A 12/1997 Fukushima et al.
 5,763,915 A 6/1998 Hshieh et al.
 5,767,550 A 6/1998 Calafut et al.
 5,776,812 A 7/1998 Takahashi et al.
 5,780,324 A 7/1998 Tokura et al.
 5,783,491 A 7/1998 Nakamura et al.
 5,783,915 A 7/1998 Shida et al.
 5,801,408 A 9/1998 Takahashi
 5,814,858 A 9/1998 Williams
 5,864,159 A * 1/1999 Takahashi 257/330
 5,879,971 A 3/1999 Witek
 5,895,952 A 4/1999 Darwish et al.
 5,930,630 A 7/1999 Hshieh et al.
 5,986,304 A 11/1999 Hshieh et al.
 5,998,836 A 12/1999 Williams
 5,998,837 A 12/1999 Williams

6,015,737 A 1/2000 Tokura et al.
 6,049,108 A 4/2000 Williams et al.
 6,121,089 A 9/2000 Zeng et al.
 6,204,533 B1 3/2001 Williams et al.
 6,221,721 B1 * 4/2001 Takahashi 438/270
 6,368,920 B1 * 4/2002 Beasom 438/270
 6,426,260 B1 * 7/2002 Hshieh 438/270
 6,429,481 B1 8/2002 Mo et al.
 6,521,497 B1 * 2/2003 Mo 438/270
 6,710,406 B1 3/2004 Mo et al.
 6,828,195 B1 * 12/2004 Mo et al. 438/270
 2002/0185679 A1 12/2002 Baliga

FOREIGN PATENT DOCUMENTS

EP 0238749 9/1987
 EP 0550770 7/1993
 EP 0583028 2/1994
 EP 0698919 2/1996
 EP 0720235 3/1996
 EP 0720236 3/1996
 EP 0720236 7/1996
 EP 0746030 12/1996
 EP 0755076 1/1997
 EP 0795911 9/1997
 EP 0801425 10/1997
 GB 2269050 1/1994
 JP 56131960 10/1981
 JP 57018365 1/1982
 JP 57153469 9/1982
 JP 58137254 8/1983
 JP 58210678 12/1983
 JP 59080970 5/1984
 JP 59193064 11/1984
 JP 60028271 2/1985
 JP 61102782 5/1986
 JP 62012167 1/1987
 JP 62016572 1/1987
 JP 62023171 1/1987
 JP 62046569 2/1987
 JP 63114173 5/1988
 JP 05226661 9/1993
 JP 08204194 8/1996
 JP 08250731 9/1996
 JP 08316479 11/1996
 JP 09036362 2/1997
 JP 09102607 4/1997
 JP 09270512 10/1997
 WO WO 93/03502 2/1993
 WO WO 95/34094 12/1995
 WO WO 97/07547 2/1997
 WO WO 97/16853 5/1997

OTHER PUBLICATIONS

Chang, T.S., et al., "Vertical FET Random-Access Memories with Deep Trench Isolation," IBM Technical Disclosure Bulletin, pp. 3683-3687 (Jan. 1980).
 Goodenough, Frank et al. "Tech Insights Enables Portable Power Control", Electronic Design, Apr. 14, 1997.
 Grant, D.A. et al., "Power Mosfets: Theory and Applications," A. Wiley-Interscience Publication COPYRIGHT. 1989, pp. 5-23. [ISBN 0-471-82867-X].
 Homes, F. E. et al., "V Groove M.O.S. Transistor Technology," Electronic Letters vol. 9, No. 19, pp. 457-458 (Sep. 20, 1973).
 Homes, F. E. et al., "VMOS—A New MOS Integrated Circuit Technology," Solid-State Electronics, vol. 17, pp. 791-797 (1974).
 Lidow, A. et al. "Power Mosfet Technology," Lidow et al., (International Electron Devices meeting, Dec. 3-5, 1979, IEAM Technical Digest, pp. 79-83).
 Lisiak, Kenneth P.; Berger, Josef. "Optimization of Nonplanar Power MOS Transistors," IEE Transactions on Electron Devices, vol. ED-25, No. 10, pp. 1229-1234 (Oct. 1978).

US 7,148,111 B2

Page 3

Ou-Yang, Paul, "Double Ion Implanted V-MOS Technology," IEEE Journal of Solid-State Circuits, vol. SC-12, No. 1, pp. 3-10 (Feb. 1977).

"Optimization of Nonplanar Power MOS Transistors," Lisiak et al., IEEE Transactions of Electron Devices, vol. ED-25, No. 10, Oct. 1975, pp. 1229-1234.

Salama, C. Andre; Oakes, James G., "Nonplanar Power Field-Effect Transistor," IEEE Transactions on Electron Devices, vol. ED-25, No. 10, pp. 1222-1228 (Oct. 1978).

Sun, S. C., "Physics and Technology of Power MOSFETs," Stanford Electronics Laboratory, Integrated Circuits Laboratory, Technical Report No. IDEZ696-1 (Feb. 1982).

Sze, S. M., "P-N-Junction Diode" Physics of Semiconductor Devices Second Edition Bell Laboratories, pp. 63-108 (1981).

* cited by examiner

U.S. Patent

Dec. 12, 2006

Sheet 1 of 9

US 7,148,111 B2

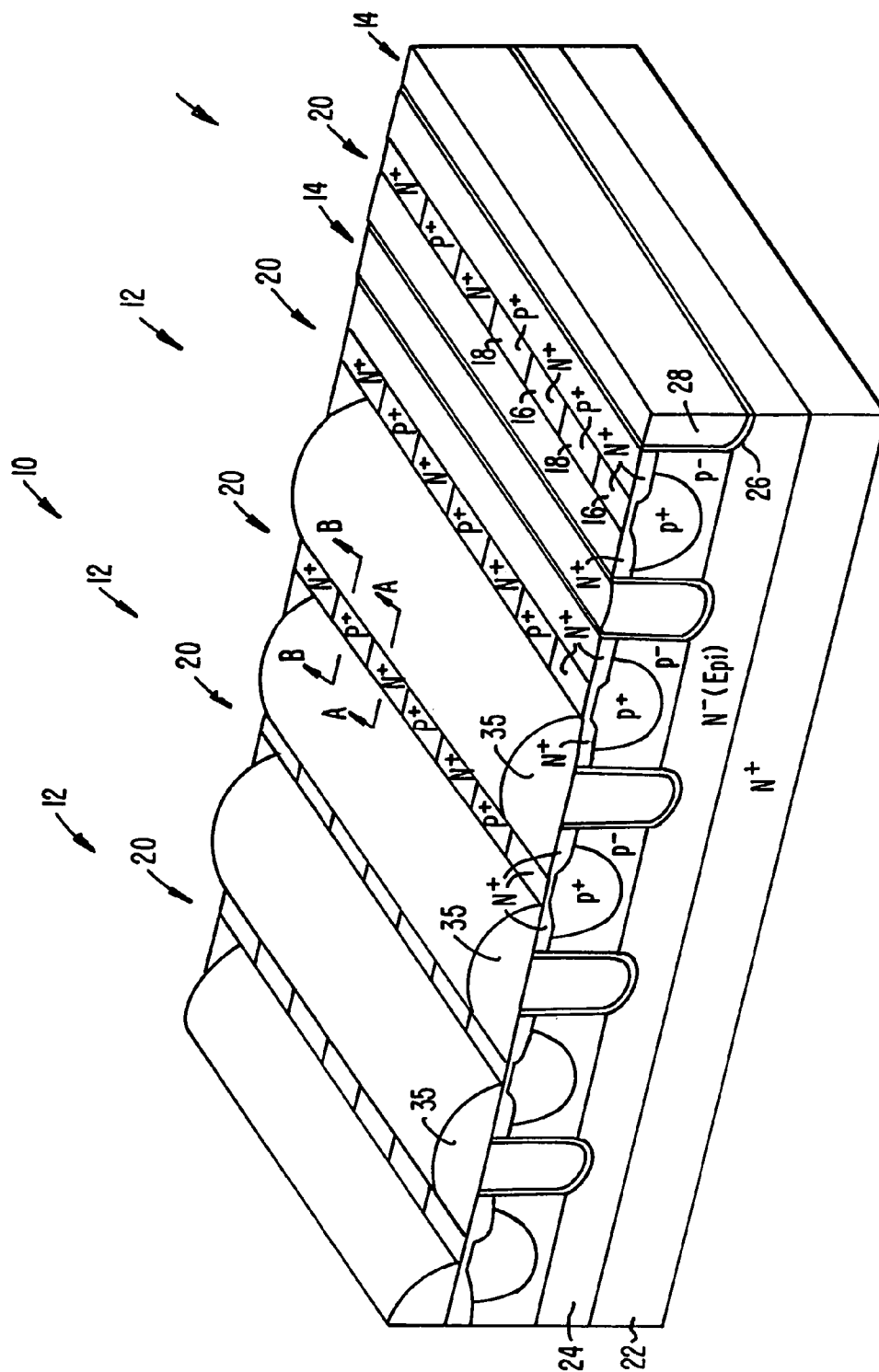


FIG. 1.

U.S. Patent

Dec. 12, 2006

Sheet 2 of 9

US 7,148,111 B2

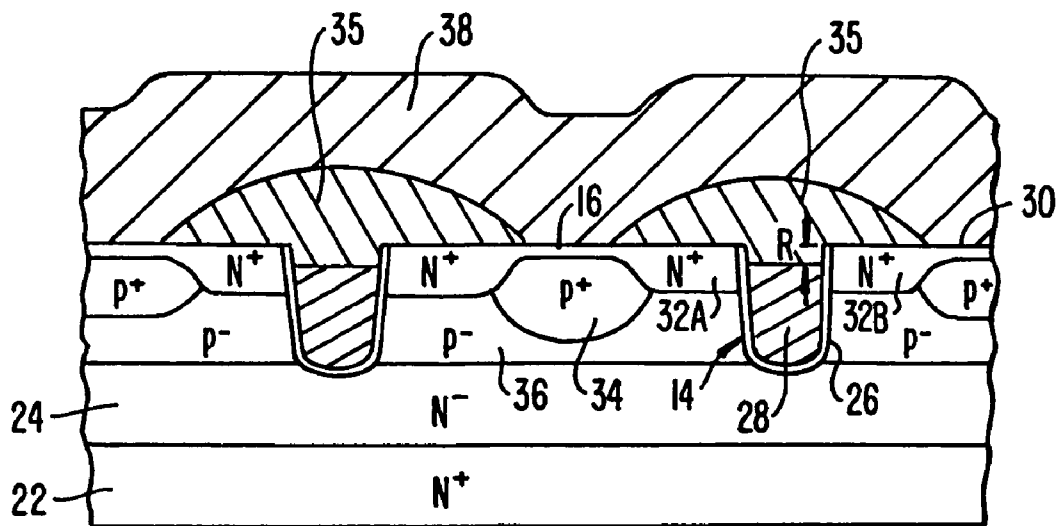


FIG. 1A.

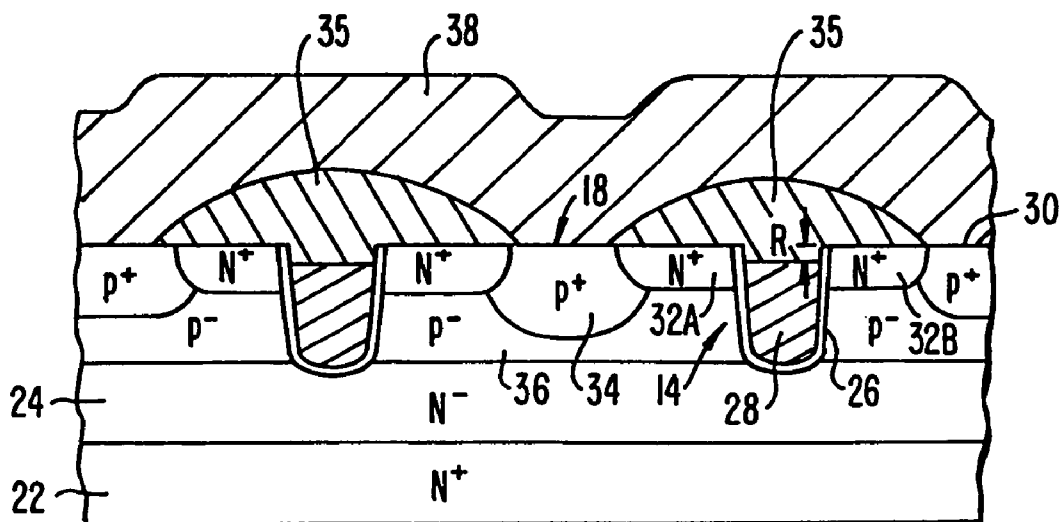


FIG. 1B.

U.S. Patent

Dec. 12, 2006

Sheet 3 of 9

US 7,148,111 B2

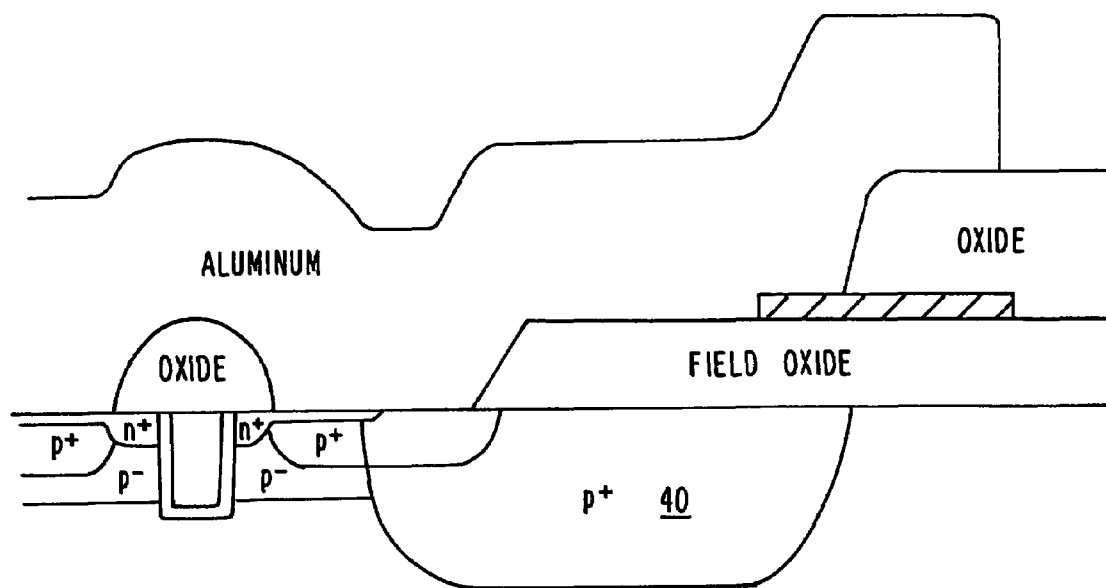


FIG. 2.

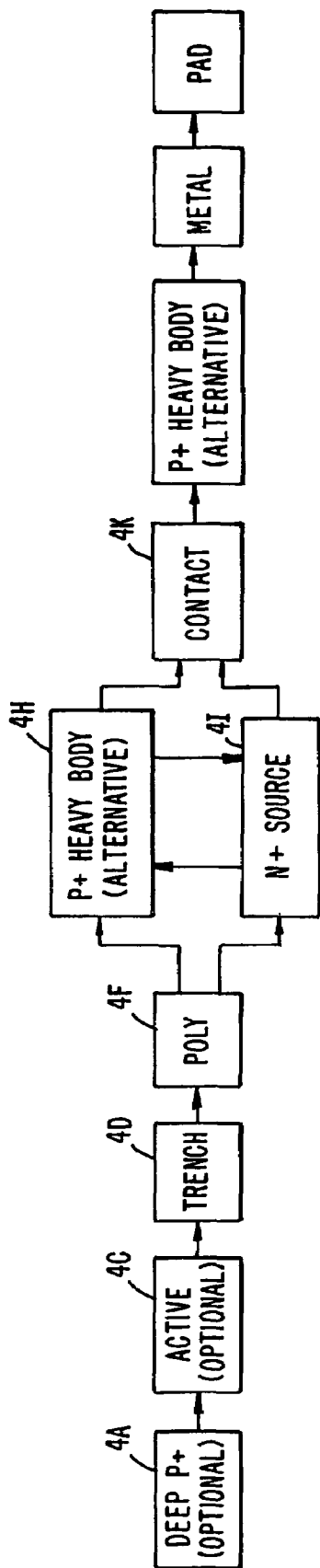


FIG. 3.

U.S. Patent

Dec. 12, 2006

Sheet 5 of 9

US 7,148,111 B2

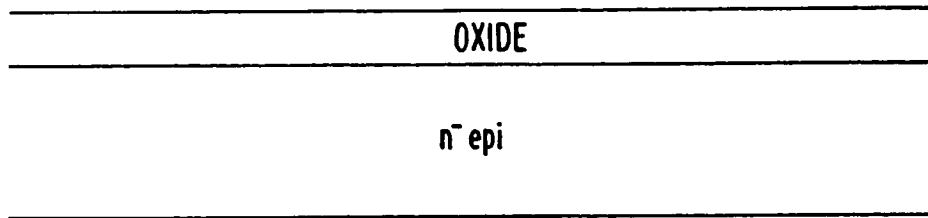


FIG. 4.

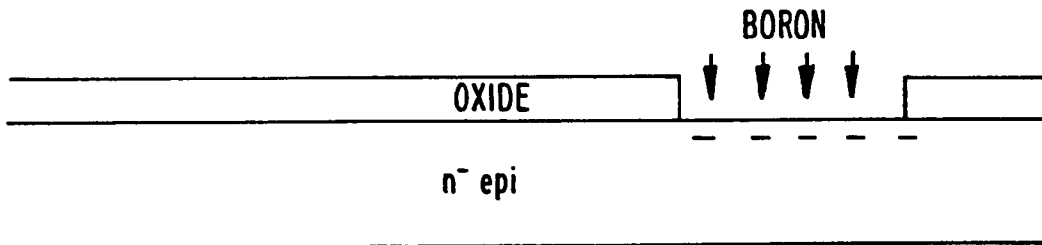


FIG. 4A.

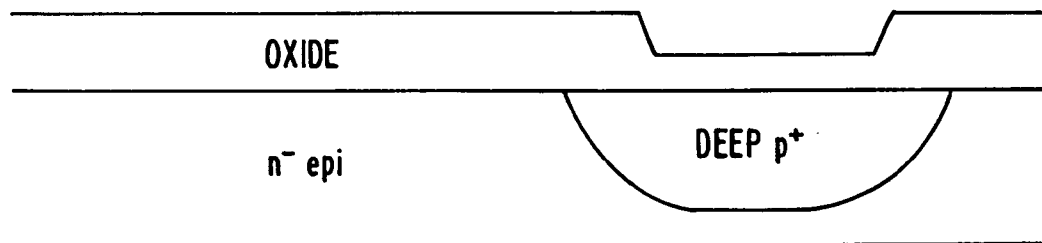


FIG. 4B.

U.S. Patent

Dec. 12, 2006

Sheet 6 of 9

US 7,148,111 B2

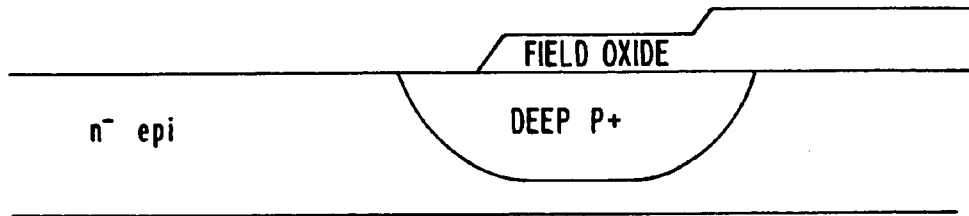


FIG. 4C.

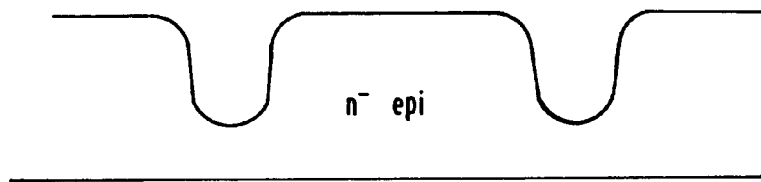


FIG. 4D.

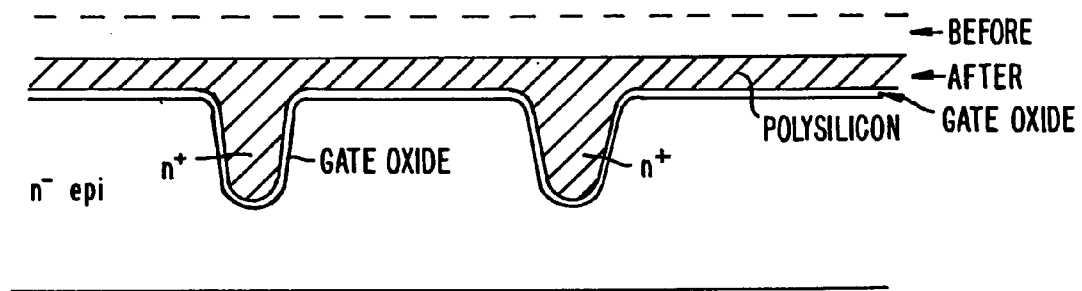


FIG. 4E.

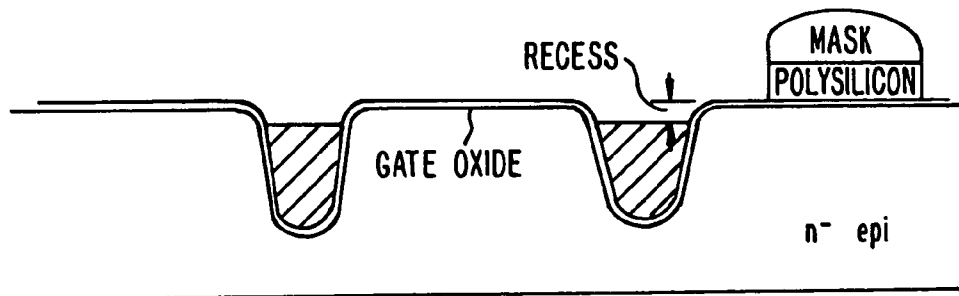


FIG. 4F.

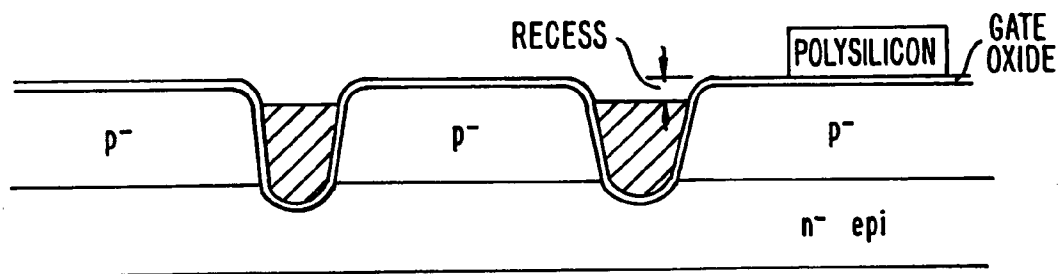


FIG. 4G.

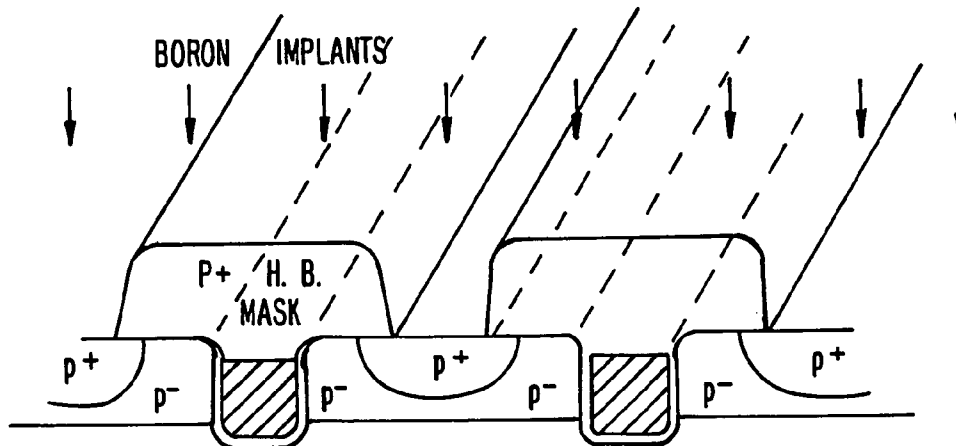


FIG. 4H.

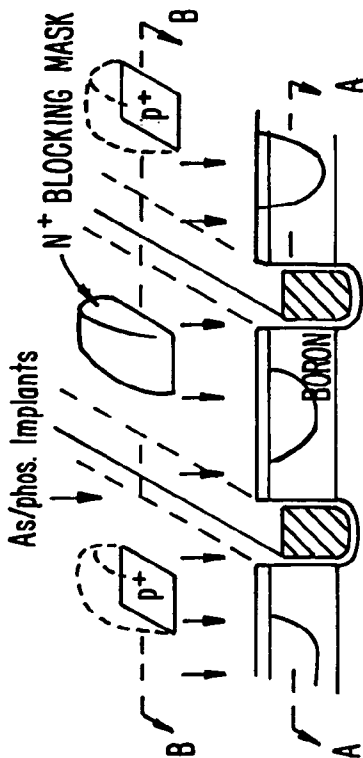
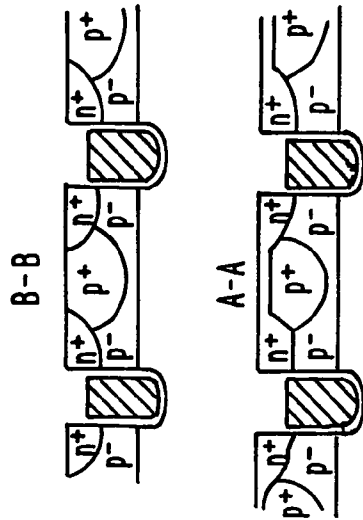


FIG. 4I.



BORON IMPLANTS (ALTERNATIVE)

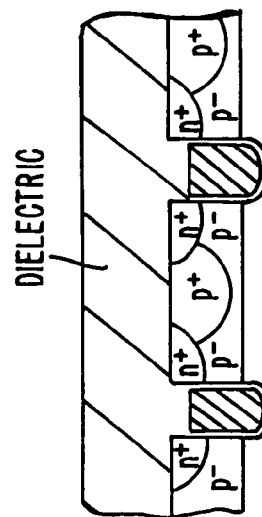


FIG. 4J.

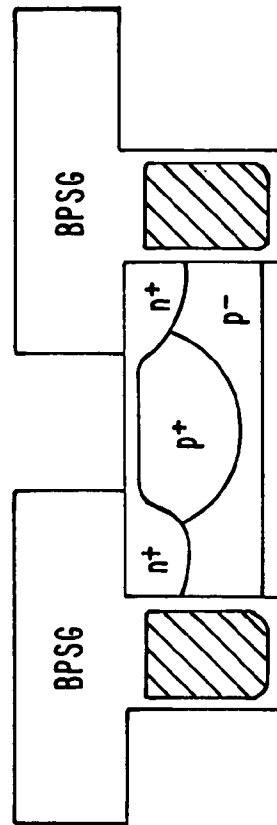


FIG. 4K.

U.S. Patent

Dec. 12, 2006

Sheet 9 of 9

US 7,148,111 B2

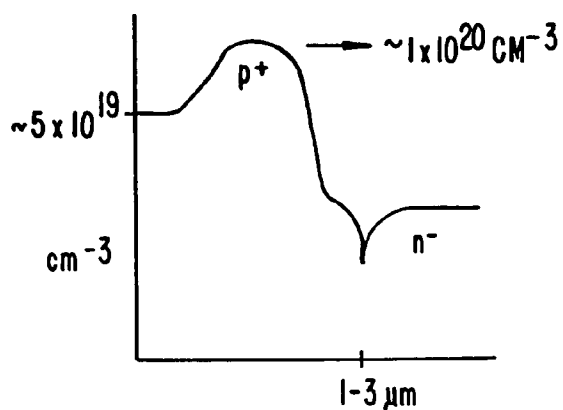


FIG. 5.

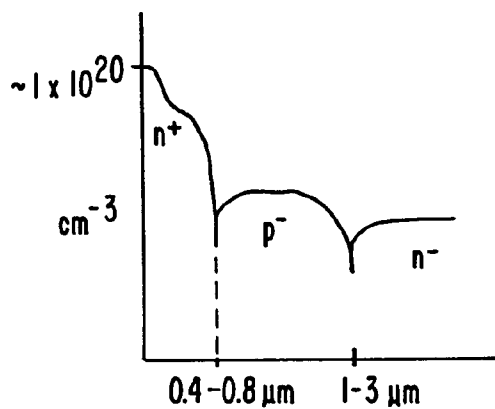


FIG. 5A.

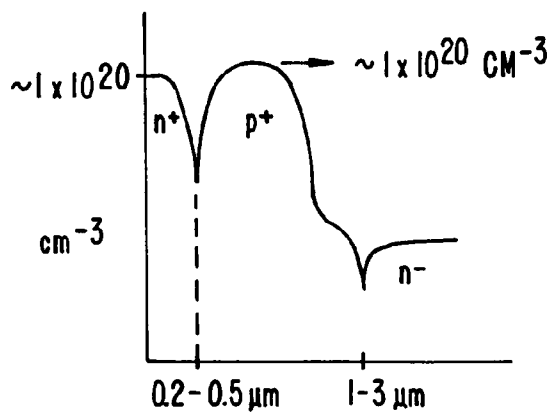


FIG. 5B.

US 7,148,111 B2

1

METHOD OF MANUFACTURING A TRENCH TRANSISTOR HAVING A HEAVY BODY REGION

This application is a continuation of and claims the benefit of U.S. application Ser. No. 10/347,254, filed Jan. 17, 2003, now U.S. Pat. No. 6,828,195, which is a continuation of U.S. application Ser. No. 09/854,102 filed May 9, 2001, now U.S. Pat. No. 6,521,497, which is a divisional of U.S. application Ser. No. 08/970,221 filed Nov. 14, 1997, now U.S. Pat. No. 6,429,481.

BACKGROUND OF THE INVENTION

The present invention relates to field effect transistors, in particular trench DMOS transistors, and methods of their manufacture.

Power field effect transistors, e.g., MOSFETs (metal oxide semiconductor field effect transistors), are well known in the semiconductor industry. One type of MOSFET is a DMOS (double diffused metal oxide semiconductor) transistor. DMOS transistors typically include a substrate on which an epitaxial layer is grown, a doped source junction, a doped heavy body, a doped well of the same (p or n) doping as the heavy body, and a gate electrode. In trench DMOS transistors the gate electrode is a vertical trench. The heavy body is typically diffused deeper than the bottom of the trench, to minimize electric field at the bottom corners of the trench and thereby prevent avalanche breakdown from damaging the device. The trench is filled with conductive polysilicon, and the polysilicon is generally overetched, to assure that it is completely removed from the surface surrounding the trench. This overetching generally leaves a recess between the top of the polysilicon and the surface of the semiconductor substrate (i.e., the surface of the epitaxial layer). The depth of this recess must be carefully controlled so that it is shallower than the depth of the source junctions. If the recess is deeper than the source junctions the source may miss the gate, resulting in high on-state resistance, high threshold, and potentially a non-functional transistor.

The source and drain junctions can be doped with either p-type or n-type dopants; in either case, the body will be doped with the opposite dopant, e.g., for n-type source and drain the body will be p-type. DMOS transistors in which the source and drain are doped with p-type carriers are referred to as "p-channel". In p-channel DMOS transistors a negative voltage applied to the transistor gate causes current flow from the source region, through a channel region of the body, an accumulation region of the epitaxial layer, and the substrate, to the drain region. Conversely, DMOS transistors, in which the source and drain are doped with n-type carriers, are referred to as "n-channel". In n-channel DMOS transistors a positive voltage applied to the transistor gate causes current to flow from drain to source.

It is desirable that DMOS transistors have low source to drain resistance ($R_{ds(on)}$) when turned on and low parasitic capacitance. The transistor structure should also avoid "punchthrough". Punchthrough occurs when, upon application of a high drain to source voltage, depletion into the body region extends to the source region, forming an undesirable conductive path through the body region when the transistor should be off. Finally, the transistor should have good "ruggedness", i.e., a high activation current is needed to turn on the parasitic transistor that inherently exists in DMOS transistors.

Generally a large number of MOSFET cells are connected in parallel forming a single transistor. The cells may be

2

arranged in a "closed cell" configuration, in which the trenches are laid out in a grid pattern and the cells are enclosed on all sides by trench walls. Alternatively, the cells may be arranged in an "open cell" configuration, in which the trenches are laid out in a "stripe" pattern and the cells are only enclosed on two sides by trench walls. Electric field termination techniques are used to terminate junctions (doped regions) at the periphery (edges) of the silicon die on which the transistors are formed. This tends to cause the breakdown voltage to be higher than it would otherwise be if controlled only by the features of the active transistor cells in the central portions of the die.

SUMMARY OF THE INVENTION

The present invention provides field effect transistors that have an open cell layout that provides good uniformity and high cell density and that is readily scalable. Preferred trench DMOS transistors exhibit low $R_{ds(on)}$, low parasitic capacitance, excellent reliability, resistance to avalanche breakdown degradation, and ruggedness. Preferred devices also include a field termination that enhances resistance to avalanche breakdown. The invention also features a method of making trench DMOS transistors.

In one aspect, the invention features a trench DMOS transistor that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of the heavy body region relative to the depths of the well and the trench is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped well has a depth less than the predetermined depth of the trench. The trench has rounded top and bottom corners. There is an abrupt junction at the interface between the heavy body and the well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface.

In another aspect, the invention features an array of transistor cells. The array includes (a) a semiconductor substrate, (b) a plurality of gate-forming trenches arranged substantially parallel to each other and extending in a first direction, the space between adjacent trenches defining a contact area, each trench extending a predetermined depth into said substrate, the predetermined depth being substantially the same for all of said gate-forming trenches; (c) surrounding each trench, a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, (d) positioned between each pair of gate-forming trenches, a doped heavy body positioned adjacent each source junction, the deepest portion of each said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches, (e) a doped well surrounding each heavy body beneath the heavy body; and (f) p+ and n+ contacts disposed at the surface of the semiconductor substrate and arranged in alternation along the length of the contact area.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise

US 7,148,111 B2

3

boron. The first energy is from about 150 to 200 keV. The first dosage is from about $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$. The second energy is from about 20 to 40 keV. The second dosage is from about $1\text{E}14$ to $1\text{E}15\text{ cm}^{-2}$.

In yet another aspect, the invention features a semiconductor die that includes (a) a plurality of DMOS transistor cells arranged in an array on a semiconductor substrate, each DMOS transistor cell including a gate-forming trench, each of said gate-forming trenches having a predetermined depth, the depth of all of the gate-forming trenches being substantially the same; and (b) surrounding the periphery of the array, a field termination structure that extends into the semiconductor substrate to a depth that is deeper than said predetermined depth of said gate-forming trenches.

Preferred embodiments include one or more of the following features. The field termination structure includes a doped well. The field termination structure includes a termination trench. The field termination structure includes a plurality of concentrically arranged termination trenches. Each of the DMOS transistor cells further comprises a doped heavy body and the doped heavy body extends into the semiconductor substrate to a depth that is less than the predetermined depth of the gate-forming trenches.

The invention also features a method of making a heavy body structure for a trenched DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into said region a second dopant at a second energy and dosage, said second energy and dosage being relatively less than said first energy and dosage.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about $1\text{E}15$ to $5\text{E}15$. The second energy is from about 20 to 40 keV. The second dosage is from about $1\text{E}14$ to $1\text{E}15$.

Additionally, the invention features a method of making a source for a trenched DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into the region a second dopant at a second energy and dosage, the second energy and dosage being relatively less than the first energy and dosage.

Preferred embodiments include one or more of the following features. The first dopant comprises arsenic and the second dopant comprises phosphorus. The first energy is from about 80 to 120 keV. The first dosage is from about $5\text{E}15$ to $1\text{E}16\text{ cm}^{-2}$. The second energy is from about 40 to 70 keV. The second dosage is from about $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$. The resulting depth of the source is from about 0.4 to 0.8 μm in the finished DMOS transistor.

In another aspect, the invention features a method of manufacturing a trenched field effect transistor. The method includes (a) forming a field termination junction around the perimeter of a semiconductor substrate, (b) forming an epitaxial layer on the semiconductor substrate, (c) patterning and etching a plurality of trenches into the epitaxial layer; (d) depositing polysilicon to fill the trenches, (e) doping the polysilicon with a dopant of a first type, (f) patterning the substrate and implanting a dopant of a second, opposite type to form a plurality of wells interposed between adjacent trenches, (g) patterning the substrate and implanting a dopant of the second type to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned above the wells, each heavy body having an

4

abrupt junction with the corresponding well, (h) patterning the substrate and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and (i) applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas.

Other features and advantages of the invention will be apparent from the following detailed description, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a highly enlarged, schematic perspective cross-sectional view showing a portion of a cell array including a plurality of DMOS transistors according to one aspect of the invention. The source metal layer and a portion of the dielectric layer have been omitted to show the underlying layers. FIGS. 1a and 1b are side cross-sectional views of a single line of transistors from the array of FIG. 1, taken along lines A—A and B—B, respectively. In FIGS. 1a and 1b the source metal and dielectric layers are shown.

FIG. 2 is a highly enlarged schematic side cross-sectional view of a semiconductor die showing a portion of the cell array and the field termination.

FIG. 3 is a flow diagram showing the photo mask sequence of a preferred process for forming a trench DMOS transistor of FIG. 1.

FIGS. 4-4K are schematic side cross-sectional views showing the individual steps of the process diagrammed in FIG. 3. The figure numbers for the detailed views in FIGS. 4-4K are shown parenthetically under the corresponding diagram boxes in FIG. 3.

FIGS. 5, 5A, and 5B are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A cell array 10, including a plurality of rows 12 of trenched DMOS transistors, is shown in FIG. 1. Cell array 10 has an open cell configuration, i.e., trenches 14 run in only one direction, rather than forming a grid. Individual cells are formed by alternating n+ source contacts 16 and p+ contacts 18 in rows 20 that run parallel to and between trenches 14. The configuration of the regions of each row that have an n+ source contact are shown in cross-section in FIG. 1A, while the regions that have a p+ contact are shown in FIG. 1B.

As shown in FIGS. 1A and 1B, each trenched DMOS transistor includes a doped n+ substrate (drain) layer 22, a more lightly doped n- epitaxial layer 24, and a gate electrode 28. Gate electrode 28 comprises a conductive polysilicon that fills a trench 14. A gate oxide 26 coats the walls of the trench and underlies the polysilicon. The top surface of the polysilicon is recessed from the surface 30 of the semiconductor substrate by a distance R (typically from about 0 to 0.4 μm). N+ doped source regions 32a, 32b are positioned one on each side of the trench 14. A dielectric layer 35 covers the trench opening and the two source regions 32a, 32b. Extending between the source regions of adjacent cells is a p+ heavy body region 34 and, beneath it, a flat-bottomed p- well 36. In the areas of the cell array which have a n+ contact 16, a shallow n+ doped contact region extends between the n+ source regions. A source metal layer 38 covers the surface of the cell array.

US 7,148,111 B2

5

The transistor shown in FIGS. 1A and 1B includes several features that enhance the ruggedness of the transistor and its resistance to avalanche breakdown degradation.

First, the depth of the p+ heavy body region 34 relative to the depths of the trench 14 and the flat bottom of the p- well is selected so that the peak electric field when voltage is applied to the transistor will be approximately halfway between adjacent trenches. The preferred relative depths of the p+ heavy body, the p- well and the trench are different for different device layouts. However, preferred relative depths can be readily determined empirically (by observing the location of peak electric field) or by finite element analysis.

Second, the bottom corners of the trench 14 are rounded (preferably, the top corners are also rounded; this feature is not shown). Corner rounding can be achieved using the process described in U.S. application Ser. No. 08/959,197, filed on Oct. 28, 1997, now U.S. Pat. No. 6,103,635. The rounded corners of the trench also tend to cause the peak electric field to be moved away from the trench corners and towards a central location between adjacent trenches.

Third, an abrupt junction at the interface between the p+ heavy body and the p-well causes the peak electric field to occur in that area of the interface. Avalanche multiplication initiates at the location of the peak electric field, thus steering hot carriers away from the sensitive gate oxide and channel regions. As a result, this structure improves reliability and avalanche ruggedness without sacrificing cell density as much as a deeper heavy body junction. This abrupt junction can be achieved by the double doping process that will be described below, or by other processes for forming abrupt junctions, many of which are known in the semiconductor field.

Lastly, referring to FIG. 2, the cell array is surrounded by a field termination junction 40 which increases the breakdown voltage of the device and thaws avalanche current away from the cell array to the periphery of the die. Field termination junction 40 is a deep p+ well, preferably from about 1 to 3 m deep at its deepest point, that is deeper than the p+ heavy body regions 34 in order to reduce the electric field caused by the junction curvature. A preferred process for making the above-described transistors is shown as a flow diagram in FIG. 3, and the individual steps are shown schematically in FIGS. 4-4K. It is noted that some steps that are conventional or do not require illustration are described below but not shown in FIGS. 4-4K. As indicated by the arrows in FIG. 3, and as will be discussed below, the order of the steps shown in FIGS. 4-4K can be varied. Moreover, some of the steps shown in FIGS. 4-4K are optional, as will be discussed.

A semiconductor substrate is initially provided. Preferably, the substrate is a N++ Si substrate, having a standard thickness, e.g., 500 μm , and a very low resistivity, e.g., 0.001 to 0.005 Ohm-cm. An epitaxial layer is deposited onto this substrate, as is well known, preferably to a thickness of from about 4 to 10 μm . Preferably the resistivity of the epitaxial layer is from about 0.1 to 3.0 Ohm-cm.

Next, the field termination junction 40 is formed by the steps shown in FIGS. 4-4C. In FIG. 4, an oxide layer is formed on the surface of the epitaxial layer. Preferably, the thickness of the oxide is from about 5 to 10 kÅ. Next, as shown in FIG. 4A, the oxide layer is patterned and etched to define a mask, and the p+ dopant is introduced to form the deep p+ well field termination. A suitable dopant is boron, implanted at an energy of from about 40 to 100 keV and a dose of $1\text{E}14$ (1×10^{14}) to $1\text{E}16$ cm^{-2} . As shown in FIG. 4B, the p+ dopant is then driven further into the substrate, e.g.,

6

by diffusion, and a field oxide layer is formed over the p+ junction. Preferably the oxide thickness is from about 4 to 10 kÅ. Finally, the oxide (FIG. 4) over the active area of the substrate (the area where the cell array will be formed) is patterned and removed by any suitable etching process, leaving only the field oxide in suitable areas. This leaves the substrate ready for the following steps that will form the cell array.

It is noted that, as an alternative to steps 4-4C, a suitable field termination structure can be formed using a ring-shaped trench which surrounds the periphery of the cell array and acts to lessen the electric field and increase the resistance to avalanche breakdown degradation. This trench field termination does not require a field oxide or deep p+ body junction to be effective. Consequently, it can be used to reduce the number of process steps. Using a trench ring (or multiple concentric trench rings) to form a field termination is described in, e.g., U.S. Pat. No. 5,430,324, the full disclosure of which is hereby incorporated herein by reference. Preferably, the trench would have substantially the same depth as the trenches in the cell array.

The cell array is formed by the steps shown in FIGS. 4D-4K. First, a plurality of trenches are patterned and etched into the epitaxial layer of the substrate (FIG. 4D). Preferably, as noted above, the trenches are formed using the process described in U.S. application Ser. No. 08/959,197, filed on Oct. 28, 1997, now U.S. Pat. No. 6,103,635, so that the upper and lower corners of each trench will be smoothly rounded. As shown in FIG. 1 and described above, the trenches are patterned to run in only one direction, defined as an open cell structure. After trench formation, a gate oxide layer is formed on the trench walls, as is well known in the semiconductor field. Preferably the gate oxide has a thickness of from about 100 to 800 Å.

Next, as shown in FIG. 4E, polysilicon is deposited to fill the trench and cover the surface of the substrate, generally to a thickness of from about 1 to 2 μm depending on the trench width (shown by the dotted lines in FIG. 4E). This layer is then planarized by the nature of its thickness relative to the trench width, typically from about 2 to 5 k Å (indicated by solid lines in FIG. 4E). The polysilicon is then doped to n-type, e.g., by conventional POCL₃ doping or by phosphorus implant. The backside of the wafer need not be stripped (as is conventionally done prior to doping the polysilicon to enhance defect gettering) because any further doping of the highly doped substrate would be unlikely to result in any enhancement in defect gettering.

The polysilicon is then patterned with a photoresist mask and etched to remove it from the trench areas, as shown in FIG. 4F. A small recess between the top of the polysilicon in the trench and the substrate surface inherently results when the polysilicon is etched completely to remove all of the polysilicon from the substrate surface. The depth of this recess must be controlled so that it does not exceed the depth of the n+ source junction that will be formed in a later step. To reduce the need to carefully control this aspect of the process, a relatively deep n+ source junction is formed, as will be discussed below.

Then, as shown in FIG. 4G, the p-well is formed by implanting the dopant, e.g., a boron implant at an energy of 30 to 100 keV and a dosage of $1\text{E}13$ to $1\text{E}15$, and driving it in to a depth of from about 1 to 3 m using conventional drive in techniques.

The next two steps (p+ heavy body formation) can be performed either before formation of the n+ source junction, or afterwards, as indicated by the arrows in FIG. 3. P+ heavy body formation and n+ source junction formation can be

US 7,148,111 B2

7

performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. 4H. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. 4K, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p- well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$, and a second boron implant at an energy of 20 to 40 keV and a dose of $1\text{E}14$ to $1\text{E}15\text{ cm}^{-2}$. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact 18. The resulting p+ heavy body junction is preferably about 0.4 to 1 μm deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5 μm deep), and includes a region of high dopant concentration near the interface with the p-well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. 5.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts 18 (FIGS. 1 and 1B), as shown in FIG. 4I. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. 4I, which correspond to FIGS. 1A and 1B).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of $5\text{E}15$ to $1\text{E}16\text{ cm}^{-2}$ followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of $1\text{E}15$ to $5\text{E}15\text{ cm}^{-2}$. The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8 μm after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n contacts 16 (see FIGS. 1 and 1A) by compensating (converting) the p-type surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. 5A and 5B respectively.

Thus, the alternating p+ and n+ contacts 18, 16, shown in FIG. 1 are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the

8

second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower $R_{ds, on}$.

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900°C ., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. 4J), after which the dielectric is patterned and etched (FIG. 4K) to define electrical contact openings over the n+ and p+ contacts 16, 18.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well known in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "n" doped instead, and vice versa.

The invention claimed is:

1. A method of manufacturing a trench transistor comprising:

providing a semiconductor substrate having dopants of a first conductivity type;

forming a plurality of trenches extending from a first surface of the substrate to a first depth into the semiconductor substrate;

lining each of the plurality of trenches with a gate dielectric material;

substantially filling each dielectric-lined trench with conductive material;

forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;

forming a source region inside the doped well and extending to a third depth that is less than the second depth, the source region having dopants of the first conductivity type; and

forming a heavy body inside the doped well, the heavy body having dopants of the second conductivity type with a peak concentration occurring at a fourth depth below the third depth of the source region and above the second depth of the doped well.

2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.

3. The method of claim 1 further comprising forming a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fourth depth that is deeper than said first depth of the trench.

US 7,148,111 B2

9

4. The method of claim 3 wherein the step of forming a deep doped region forms a PN junction diode with the substrate that helps improve a breakdown voltage of the transistor.

5. The method of claim 3 wherein the deep doped region forms a termination structure around the periphery of the substrate.

6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.

7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.

8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.

9. The method of claim 8 wherein the double implant process comprises:

a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body; and

a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.

10. The method of claim 9 wherein the first implant occurs at approximately the fourth depth.

11. The method of claim 9 wherein the first energy level is higher than the second energy level.

12. The method of claim 11 wherein the first dosage is higher than the second dosage.

13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.

14. The method of claim 1 wherein the step of forming the heavy body comprises using a continuous dopant source at the surface of the semiconductor substrate.

15. The method of claim 1 wherein the step of forming a plurality of trenches comprises patterning and etching the plurality of trenches that extend in parallel along a longitudinal axis.

16. The method of claim 15 further comprising forming a contact area on the surface of the substrate between adjacent trenches.

17. The method of claim 16 wherein the step of forming the contact area comprises forming alternating source contact regions and heavy body contact regions.

18. The method of claim 16 wherein the step of forming the contact area comprises forming a ladder-shaped source contact region surrounding heavy body contact regions.

19. The method of claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises:

forming a source blocking mask on the surface of the semiconductor substrate patterned to cover the heavy body contact regions; and

implanting dopants of the first conductivity type to form the ladder-shaped source contact region.

20. The method of claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises forming a dielectric layer on the surface of the semiconductor substrate patterned to expose the heavy body contact regions.

21. The method of claim 1 wherein the source region is formed prior to the heavy body.

22. The method of claim 1 wherein the step of providing a semiconductor substrate comprises:

forming a drain contact region at a second surface opposite to the first surface of the substrate; and

forming a substantially uniformly doped epitaxial layer atop said drain contact region.

10

23. A method of manufacturing a trench transistor comprising:

providing a semiconductor substrate having dopants of a first conductivity type;

forming a plurality of trenches extending from a first surface of the substrate to a first depth into the semiconductor substrate;

lining each of the plurality of trenches with a gate dielectric material;

substantially filling each dielectric-lined trench with conductive material;

forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;

forming a source region inside the doped well to a third depth, the source region having dopants of the first conductivity type; and

forming a heavy body inside the doped well to a fourth depth between the third depth of the source region and the second depth of the doped well, the heavy body having dopants of the second conductivity type with a dopant concentration that is higher near the interface with the doped well than near the first surface.

24. The method of claim 23 further comprising forming a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fifth depth that is deeper than said first depth of the trench.

25. The method of claim 24 wherein the step of forming a deep doped region forms a PN junction diode with the substrate that helps improve a breakdown voltage of the transistor.

26. The method of claim 24 wherein the deep doped region forms a termination structure around the periphery of the substrate.

27. The method of claim 23 wherein the source region is formed prior to the heavy body.

28. The method of claim 23 wherein the step of providing a semiconductor substrate comprises:

forming a drain contact region at a second surface opposite to the first surface of the substrate; and

forming a substantially uniformly doped epitaxial layer atop said drain contact region.

29. A method of manufacturing a trench transistor comprising:

providing a semiconductor substrate having dopants of a first conductivity type, the semiconductor substrate including a first highly doped drain layer and a second more lightly and substantially uniformly doped epitaxial layer atop and adjacent the first layer;

forming a plurality of trenches extending to a first depth into the epitaxial layer, the plurality of trenches creating a respective plurality of epitaxial mesas;

lining each of the plurality of trenches with a gate dielectric material;

substantially filling each dielectric-lined trench with conductive material;

forming a plurality of doped wells in the plurality of epitaxial mesas, respectively to a second depth that is less than said first depth of the plurality of trenches, the plurality of doped wells having dopants of a second conductivity type opposite to said first conductivity type;

forming a plurality of source regions adjacent the plurality of trenches and inside the plurality of doped wells, the source regions having a third depth and dopants of the first conductivity type;

US 7,148,111 B2

11

forming a plurality of heavy body regions each inside a respective one of the plurality of doped wells, each heavy body region having a fourth depth between the third depth of the source region and the second depth of the doped well, and having dopants of the second conductivity type; and

adjusting a dopant profile of the plurality of heavy body regions so that peak electric field is moved away from a nearby trench toward the heavy body resulting in avalanche current that is substantially uniformly distributed.

30. The method of claim **29** wherein the step of forming the plurality of heavy body regions comprises a double implant process.

31. The method of claim **30** wherein the double implant process comprises:

a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body; and

12

a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.

32. The method of claim **31** wherein the first implant occurs at approximately the fourth depth.

33. The method of claim **31** wherein the first energy level is higher than the second energy level.

34. The method of claim **33** wherein the first dosage is higher than the second dosage.

35. The method of claim **29** wherein the step of forming the plurality of heavy body regions comprises a process of diffusing dopants of the second conductivity type.

36. The method of claim **29** wherein the step of forming the plurality of heavy body regions comprises using a continuous dopant source at the surface of the semiconductor substrate.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,148,111 B2
APPLICATION NO. : 10/927788
DATED : December 12, 2006
INVENTOR(S) : Brian Sze-Ki Mo et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

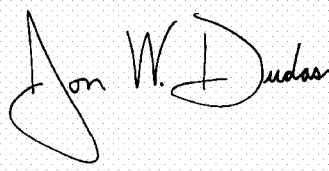
Title Page

In the Assignee information (73):

“San Jose, CA” should be --South Portland, ME--.

Signed and Sealed this

Sixth Day of March, 2007

A handwritten signature in black ink on a light gray dotted background. The signature is written in a cursive style and reads "Jon W. Dudas".

JON W. DUDAS

Director of the United States Patent and Trademark Office

EXHIBIT F

(12) **United States Patent**
Grebs et al.

(10) **Patent No.:** **US 6,818,947 B2**
(45) **Date of Patent:** **Nov. 16, 2004**

(54) **BURIED GATE-FIELD TERMINATION STRUCTURE**

(75) Inventors: **Thomas E. Grebs**, Mountaintop, PA (US); **Christopher B. Kocon**, Plains, PA (US); **Rodney S. Ridley, Sr.**, Mountaintop, PA (US); **Gary M. Dolny**, Mountaintop, PA (US); **Nathan Lawrence Kraft**, Wilkes-Barre, PA (US); **Louise E. Skurkey**, Conyngham, PA (US)

(73) Assignee: **Fairchild Semiconductor Corporation**, South Portland, ME (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/247,464**

(22) Filed: **Sep. 19, 2002**

(65) **Prior Publication Data**

US 2004/0056302 A1 Mar. 25, 2004

(51) **Int. Cl.**⁷ **H01L 29/76**

(52) **U.S. Cl.** **257/330; 257/329; 257/331; 257/332; 438/259; 438/270; 438/271; 438/589**

(58) **Field of Search** **257/302-339**

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,876,579 A 10/1989 Davis et al.

5,233,215 A 8/1993 Baliga
5,578,851 A 11/1996 Hshieh et al.
5,605,852 A 2/1997 Bencuya
5,639,676 A 6/1997 Hshieh et al.
6,110,763 A 8/2000 Temple
6,188,105 B1 2/2001 Kocon et al.
6,362,026 B2 3/2002 Zeng et al.

OTHER PUBLICATIONS

B. Jayant Baliga, Power Semiconductor Devices, Chapter 3: Breakdown Voltage; Section 3.6, Edge Terminations, pp. 81-112, PWS Publishing Company, Boston, MA, Copyright 1996.

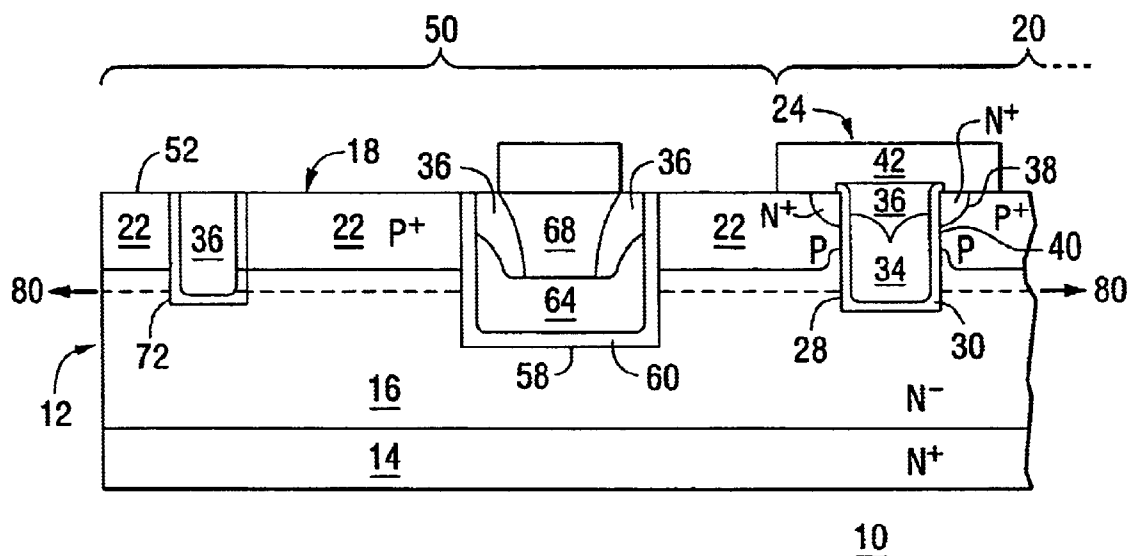
Primary Examiner—Fetsum Abraham

(74) *Attorney, Agent, or Firm*—Laurence S. Roach, Esq.; Law Office of Thomas R. FitzGerald

(57) **ABSTRACT**

In a power semiconductor device **10**, a continuous trench has an outer circumferential portion **58** that includes a field plate and inner portions **28** that carry include one or more gate runners **34** to that the gate runners and the field plate are integral with each other. The trench structure **58**, **28** is simpler to form and takes up less surface space that the separate structures of the prior art. The trench is lined with an insulator and further filled with conductive polysilicon and a top insulator.

10 Claims, 5 Drawing Sheets



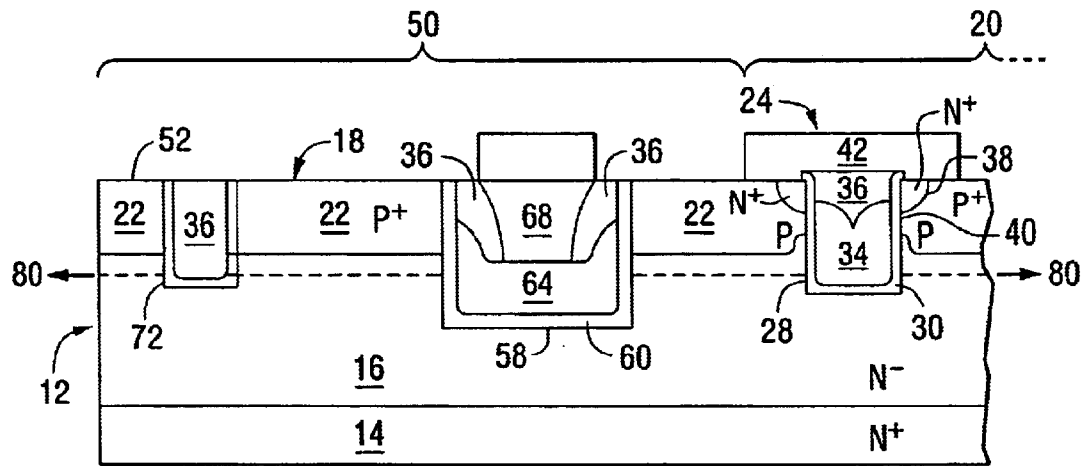


FIG. 1

10

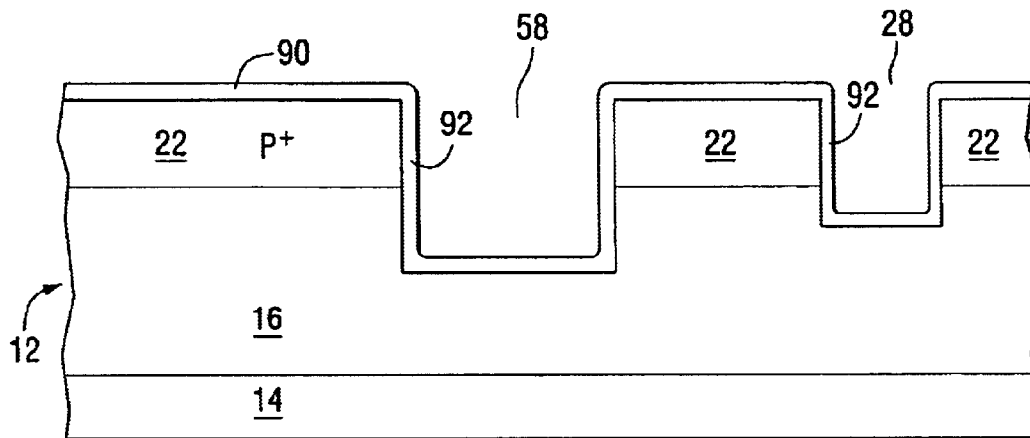
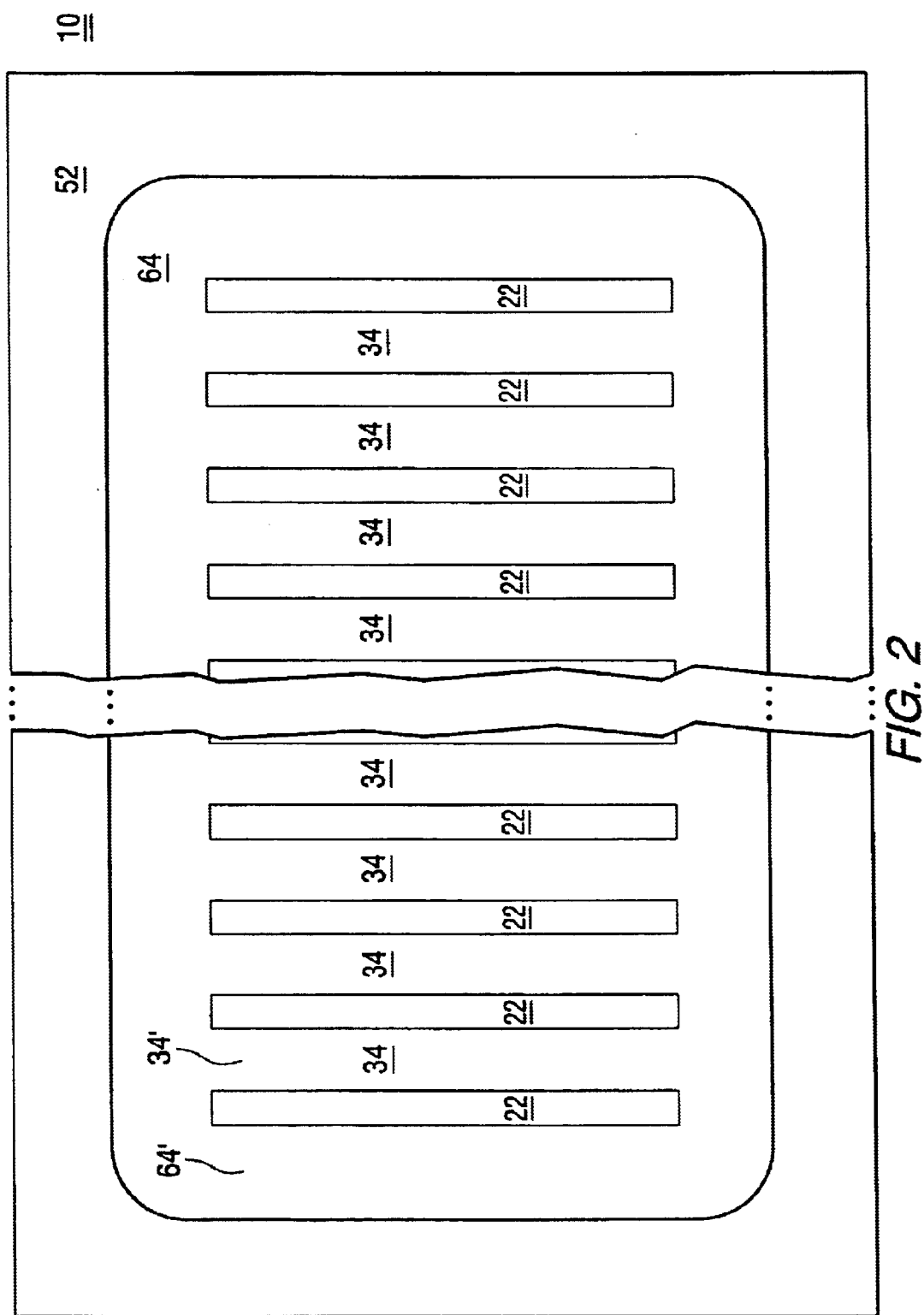


FIG. 3A



U.S. Patent

Nov. 16, 2004

Sheet 3 of 5

US 6,818,947 B2

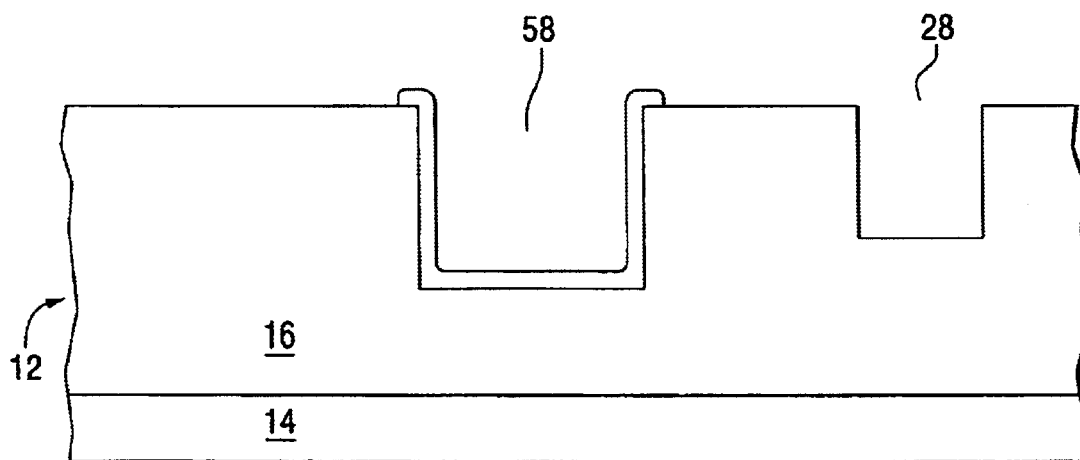


FIG. 3B

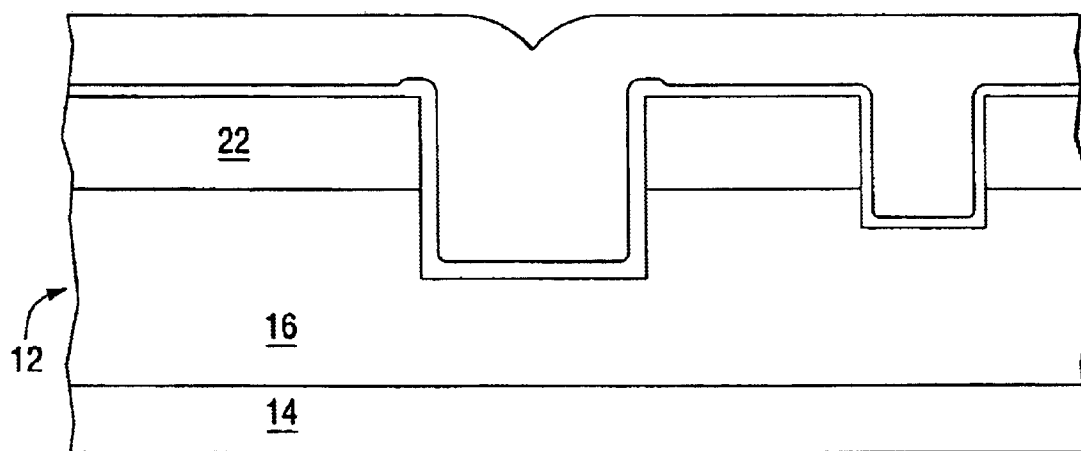


FIG. 3C

U.S. Patent

Nov. 16, 2004

Sheet 4 of 5

US 6,818,947 B2

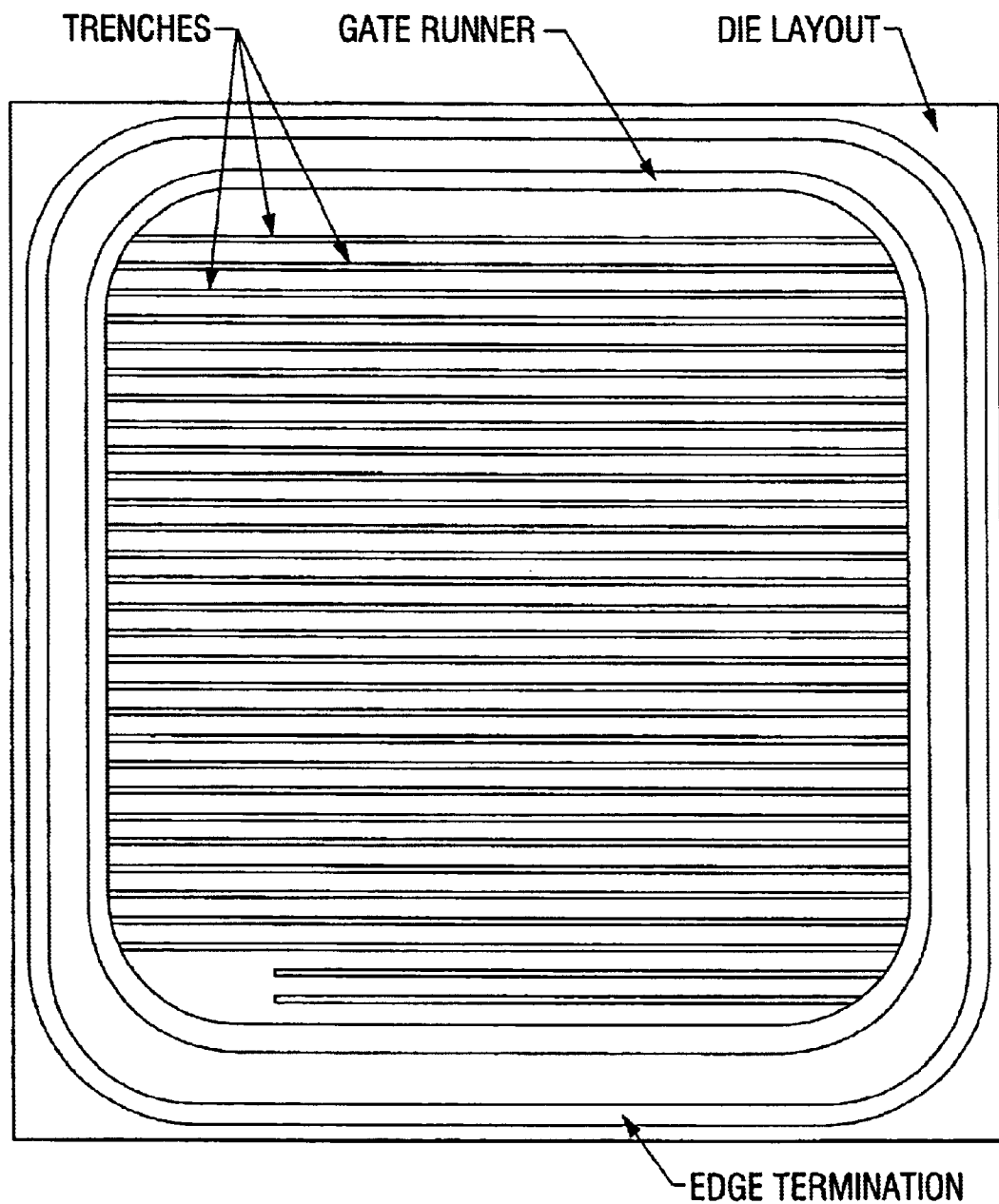


FIG. 4A

U.S. Patent

Nov. 16, 2004

Sheet 5 of 5

US 6,818,947 B2

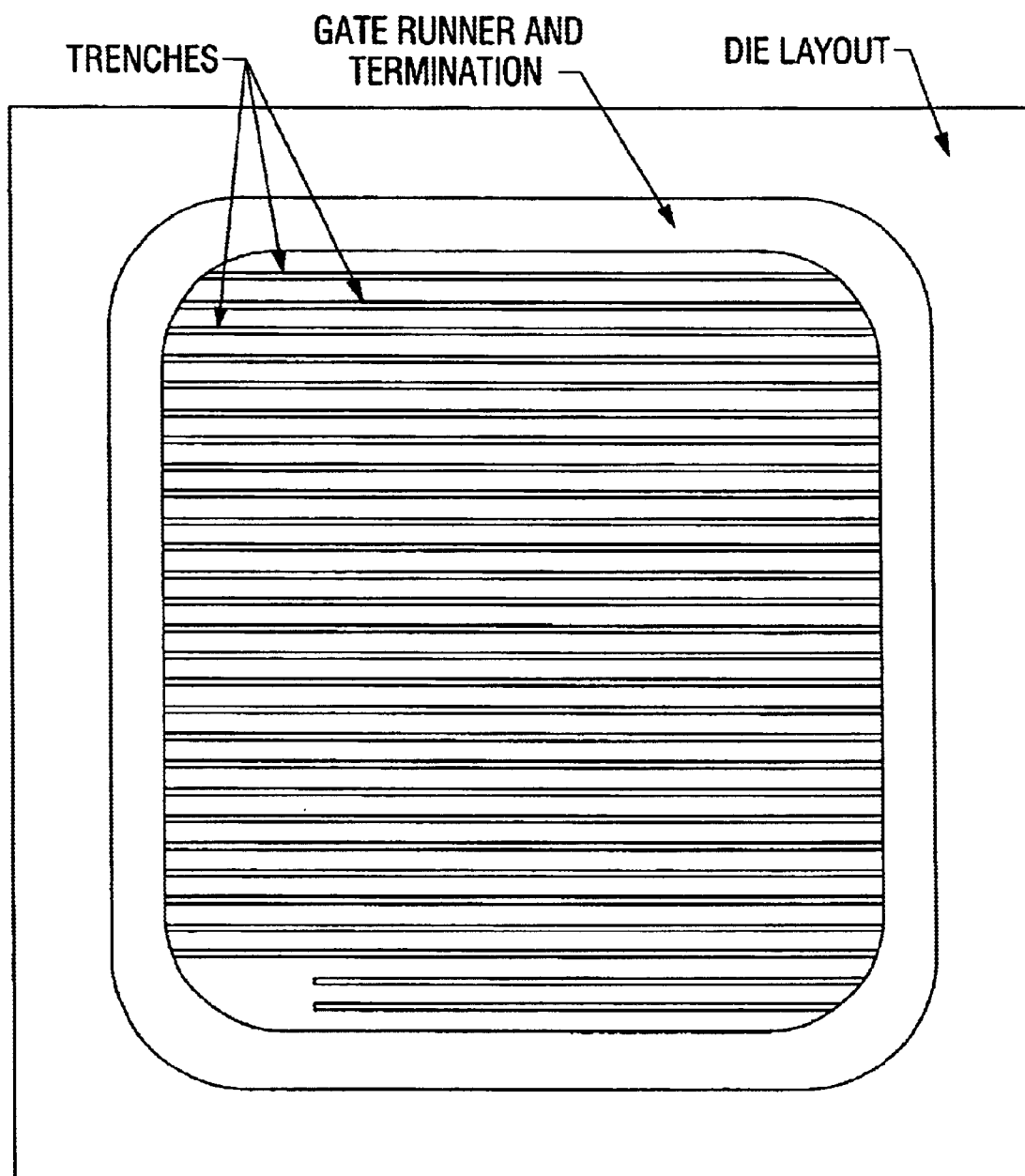


FIG. 4B

US 6,818,947 B2

1

**BURIED GATE-FIELD TERMINATION
STRUCTURE****FIELD OF THE INVENTION**

This invention relates to semiconductor devices and, more particularly, to semiconductor power devices and methods for fabricating such devices.

BACKGROUND OF THE INVENTION

There continues to be a growing demand for power switching devices, i.e., transistor devices capable of carrying large currents at high voltages. Such devices include bipolar and field effect devices including, for example, the Insulated Gate Bipolar transistor (IGBT) and the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Desirable characteristics of such devices include low on-resistance, fast switching speeds and low current draw during switching operations. That is, it is desirable to switch from an "off" state to an "on" state by applying a bias voltage to the gate electrode while experiencing only a small amount of current flow based on minimal capacitance inherent to the gate structure.

Notwithstanding significant advances in power device technologies, there remains a need to provide still higher-performing and more cost-efficient devices. For example, it is desirable to further increase current density relative to the total die area of a device. One of the limiting factors to higher current ratings is the breakdown voltage, particularly in the edge termination region. That is, because semiconductor junctions are not infinitely parallel, but include curvature, numerous techniques are employed to avoid otherwise high concentrations of electric field lines. Absent inclusion of so-called edge-termination designs, e.g., field rings, channel stop implants and field plates, to overcome degradation in the breakdown voltages, it would not be possible to approach the theoretical breakdown voltage of a semi-infinite junction. However, it is undesirable that, conventionally, a significant portion of the device die area must be devoted to edge termination designs in order to address this problem.

Breakdown voltage phenomena are well understood and the literature is replete with examples of edge termination designs. See, for example, see Ghandhi, *Semiconductor Power Devices*, John Wiley & Sons, Inc., 1977 (ISBN 0-471-029998), incorporated herein by reference, which discusses this subject at chapter two. See, also, Baliga, *Modern Power Devices*, Krieger Publishing Company, Malabar, Fla., 19920 (ISBN0894647997), also incorporated herein by reference, which provides relevant discussion at chapter three. In addition to conventional field rings and field plates, trenched field plates have been considered for edge termination applications. U.S. Pat. No. 5,233,215 discloses use of one or more trenched, floating field plates in combination with field rings in order to terminate a silicon carbide MOSFET. U.S. Pat. No. 5,578,851 discloses field rings separated by trenches, allowing the field rings to be closely spaced in order to conserve area. The trenches may be filled with polysilicon electrically connected to the MOSFET gate electrode. Nonetheless trench termination structures continue to occupy significant portions of the device die area and there is a need to provide termination techniques which are more area efficient. It is also desirable to reduce the manufacturing costs associate with high voltage performance. These and other benefits will be apparent from the invention that is now described.

2

SUMMARY OF THE INVENTION

An improved semiconductor power device is now provided. In one embodiment of the invention the device includes a semiconductor layer having a transistor region including a source/drain formation and a termination region surrounding the transistor region. The termination region includes an outer periphery corresponding to an edge of the device. A conductor, configured for connection to a voltage supply, includes first and second conductor portions. The first conductor portion is positioned in the transistor region to control current flow through the source/drain formation and the second conductor portion is positioned in the termination region. The second conductor portion includes a contact for connection to the voltage supply and a feed comprising conductive material formed in a trench extending along the outer periphery and around the transistor region. The feed portion electrically connects the contact portion with the first conductor portion.

An exemplary device according to the invention includes a layer of semiconductor material having an active device region and a peripheral region surrounding the active region. A transistor device formed in the active region has a gate region including a gate conductor formed in a trench. The gate conductor is electrically isolated from the semiconductor layer by a relatively thin insulator. A second trench is formed along the peripheral region and includes a second conductor formed therein with a relatively thick insulator positioned to electrically isolate the second trench conductor from the semiconductor layer.

An associated method for manufacturing a semiconductor device includes providing on a layer of semiconductor material an active region and a termination periphery region surrounding the active region with a trenched transistor formation in the active region. A trenched gate runner is formed in the termination region along the active region.

A method for operating a semiconductor device includes providing a semiconductor layer with an active transistor region and a trenched field plate positioned about the transistor region for increasing breakdown voltage. The field plate operates as a conductive feed to control switching of transistors in the active region. As such, the invention reduces the number of elements needed to make a power transistor by combining the gate runners and the field plate into one structure. The invention thus reduces the number of steps needed to make a device. Likewise, it increases the effective useable area of substrate so that substrates made with the invention can handle larger currents.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more fully understood when the following detailed description is read in conjunction with the drawings wherein:

FIG. 1 is a partial view in cross section of a semiconductor device incorporating the invention;

FIG. 2 is a plan view taken of the FIG. 1 device;

FIGS. 3A–3C illustrate a sequence of fabrication steps according to the invention;

FIGS. 3A–3C illustrate a sequence of fabrication steps according to the invention;

FIG. 4A is a to view of prior art using planar edge termination and gate runner structures;

FIG. 4B is a to view of the invention using buried termination and gate runner structures.

In accord with common practice the various illustrated features in the drawings are not to scale, but are drawn to

US 6,818,947 B2

3

emphasize specific features relevant to the invention. Moreover, the sizes of features and the thicknesses of layers may depart substantially from the scale with which these are shown. Reference characters denote like elements throughout the figures and the text.

DETAILED DESCRIPTION OF THE INVENTION

The partial cross sectional view of FIG. 1 illustrates a P-channel MOSFET device 10 formed in a semiconductor layer 12, including N+ lower layer 14 and N- upper layer 16 which may, for example, be epitaxially grown. The layer 16 has an upper surface 18. A P+ diffusion region 22 extends from the surface 18 into the upper layer 16. An active transistor region 20 of the device 10 (right side of drawing) includes a repetitive pattern of MOS cell structures each having a vertical source/drain formation. For simplicity of illustration only one exemplary MOSFET cell 24 is shown extending through a body region portion of the diffusion region 22. The device 10 will include many MOSFET cells, although the specific design of the cell 24 is exemplary the invention is not at all limited to any particular type of cell design nor limited solely to MOSFET devices.

The cell 24 comprises a trench 28, conventionally lined with a thermally grown gate oxide layer 30 having thickness in the range of 800 to 1200 Angstroms (80 to 120 nm). The trench may have a depth on the order of 1.5 to 3 microns with a width of one to two microns and is substantially filled with conductive material, e.g., doped polysilicon, to form a conductive gate electrode 34. The balance of the trench opening is conventionally filled with deposited insulator 36 which may, for example, be borophosphosilicate glass (BPSG). N+ source region 38 is formed along the surface 18 in an upper portion of the layer 16 surrounding the trench 28. Lightly P-doped channel region 40 is formed in the otherwise more heavily doped diffusion region 22, between the source region 38 and that portion of the N- layer 16 along the trench 28 which forms the drift region of the cell 24. The oxide layer 30 provides electrical isolation between the gate electrode 34 and each of the source region 38, channel region 40 and N- layer 16 (drain), allowing a conductive inversion layer to form in the channel region 40 when a voltage is applied to the gate electrode 34 relative to the source region 38. A source contact 42, e.g., Al, is provided for connection to the P+ region 22 as well as the source region 38 in order to suppress parasitic NPN bipolar effects which could occur under forward bias conditions, i.e., with the combination of the N+ region 38, the P+ region 22 and the N-type layers 14 and 16.

Still referring to FIG. 1, a termination region 50 (left side of drawing) extends from the active region 20 to the outer periphery 52, i.e., the die edge, of the device 10. A gate runner trench 58 having depth and width substantially larger than that of the trench 28 is formed through the P+ region 22 in the termination region 50. It may, for example, be 3 to 6 microns deep and 3 to 5 microns wide, but the trench 58 could be made substantially larger based on the desired device characteristics. The trench 58 is lined with a relatively thick insulative layer 60, e.g., 1.5 or more times the thickness of the gate oxide layer 30 and, preferably, at least 300 to 500 nm.

Preferably, initial portions of the insulative layer 60 are formed before the gate oxide layer 30 is formed, but the layer 60 may include the thermally grown layer 30 as a component thereof. Preferably the insulative layer 60 predominantly comprises thermally grown or deposited silicon

4

oxide, but may be formed with other dielectric materials. The trench 58 is substantially filled with conductive material 64, and if this is the same deposit of doped polysilicon which forms the conductive gate electrode 34, then the gate electrode 34 and the conductive material 64 will be integrally formed and a continuous layer, although they each may retain different functionalities. The remaining upper portion of the trench 58 is lined with the deposited insulator 36, e.g., BPSG and a metal contact 68, preferably Al, is formed thereover.

The diffusion region 22 extends from the active region 20, through the termination region to the die edge. An isolation trench 72, which may be formed at the same time as the trench 28, includes the thermally grown oxide layer 30 and the deposited insulator 36, preferably BPSG.

FIG. 2 is a simplified plan view of the device 10 taken along the cut-line 80 of FIG. 1, illustrating a combination of an exemplary pattern of the trenched conductive material 64 and an exemplary pattern the trenched gate electrode 34. For the FIG. 2 embodiment the partial view of FIG. 1 corresponds to a cross section taken through an end-most trenched gate electrode 34, referenced in the drawing as 34' and through the adjacent portion of the conductive material 64, referenced in the drawing as 64'. It should be recognized that, for each illustrated gate electrode 34 in FIG. 2, there is a corresponding MOS cell structure (not illustrated in FIG. 2) such as a MOSFET cell 24. For purposes of illustration the gate electrodes 34 of only a few trenches 28 of the device 10 are shown, and neither the outline of the trenches 28 nor the gate oxide layers 30 are shown in FIG. 2. A typical power device may include many more trenched gate electrodes than illustrated in the figures.

In the FIG. 2 embodiment the trenched conductive material 64 extends along the die edge 52 to provide a field plate termination. The isolation trench 72 (not shown in FIG. 2) may also extend along the die edge 52. With a metal contact (such as the contact 68 of FIG. 1) connecting a gate voltage supply with the conductive material 64, the conductive material 64 may be integrally formed in connection with the gate electrodes 34 to feed the gate signal to each MOSFET cell 24. Thus the trench 58 with conductive material 64 also serves as the gate runner, in order to feed the external gate supply to each of multiple electrodes 34. A feature of the invention is provision of one trenched conductor to serve as both a field plate and a gate runner to the several MOS cells in a device structure.

An exemplary method of making the device 10 is illustrated in FIGS. 3A-3D, showing primarily those steps relevant to formation of the trenches 28 and 58. Other conventional steps and process details for formation of power switching devices are not described as these will be readily apparent to those skilled in the art.

With reference to FIG. 3A, the method for fabricating the device 10 is illustrated beginning with the semiconductor layer 12 shown to have the N+ lower layer 14 and N- upper layer 16 formed therein. A conventional P+ implant has been made through the surface 18, and is shown after diffusion to create the P+ region 22. A low-temperature silicon oxide 90 is formed over the eventual surface 18 followed by a conventional pattern and etch to form the trenches 28 and 58. If it is desired to have the trenches 58 extend deeper into the layer 12, e.g., substantially further into the N- upper layer 16 than the trenches 28, then separate pattern and etch steps are had to create this feature. The trenches are shown lined with a sacrificial thermal oxide layer 92.

Referring next to FIG. 3B, once the trenches are defined, it is preferable to simultaneously remove both the low-

US 6,818,947 B2

5

temperature oxide layer **90** and the sacrificial thermal oxide layer **92**, e.g., by a wet etch. Next, the trenches **28** are masked so that the thick layer **60** of silicon oxide, e.g., deposited by chemical vapor deposition (CVD), is selectively formed in the trenches **58** without formation of the same oxide in the trenches **28**. Alternately, the thick oxide layer **60** may be formed overall and selectively removed from the trenches **28** by a pattern and etch process.

After the thick oxide layer **60** is defined in the trench **58** (and subsequent to removal of any masking from over the trenches **28** or **58**, the high quality thermal gate oxide layer **30** is grown to a thickness on the order of 100 nm. Although the gate oxide layer **30** is intended primarily for formation in the trenches **28**, it may also be formed in the trenches **58** to add to the thickness of the layer **60**. The interim structure is shown in FIG. 3C with a polysilicon layer **96** deposited by CVD, which is subsequently patterned to form the gate electrode **34** and conductive material **64** of trench **58** as shown in FIG. 1. Subsequent process steps are conventional and need not be separately illustrated to describe the formation of other features shown in FIG. 1. After formation of the contacts **42** and **68** as shown for the structure of FIG. 1 conventional insulator is applied over the exposed surface.

An advantage of the invention is that the edge termination feature, e.g., the trench **58**, need not be separately formed. Rather, definition of a termination trench with the same lithography steps as the trench **28** avoids raised topology effects which can otherwise obscure smaller feature definition. With the invention it is now possible to reduce the spacing between the active trenches **28** and the termination region **50** without experiencing adverse lithographic effects such as a reduction in the width of a trench **28** formed immediately next to a trench **58**.

FIG. 4A shows a top view of the prior art using planar edge termination and gate runner structures. FIG. 4B shows the top view of the invention using buried termination and gate runner structures. By integrating the termination structure with the gate runner structure there is a reduction in the total die area required to effect both of these functions. For example, the distance from the die edge periphery **52** to the first active trench **28** may be about 20 microns, while for a device of similar rating but with a conventional edge termination structure, the distance from the edge of the die to the first active trench will be on the order of 120 microns. Also, having the termination region **50** include a portion of region **22** there is no need for a separate implant step, this resulting in a reduction in the number of processing steps required for manufacture of the device. With the termination structure formed in a trench that is simultaneously formed with the gate oxide trench, the overlying surface topography is planar, i.e., not characterized by steps due to oxide formation, and this avoids puddling of photoresist which is known to compromise lithographic image integrity.

Generally, the invention enables a higher breakdown voltage at the die edge with a reduced number of process steps. Although the invention has been described for a particular device type, the concepts apply to edge termination design for a wide variety of devices types and there is no limit on the voltage range of devices with which the invention may be practiced. The design principles may be readily applied to prevent breakdown voltages well in excess of 200 volts.

An architecture and process have been described for an improved semiconductor device. Exemplary embodiments have been disclosed while other embodiments of the invention, including structures composed of compound

6

semiconductor materials, will be apparent. It is also to be understood that when a layer has been described or illustrated as positioned on or over another layer, there may be another intervening layer (not illustrated) associated with the same or an alternate embodiment of the invention. Moreover, although the invention has been illustrated for one set of conductivity types, e.g., N channel devices, application of the invention is contemplated for opposite conductivity-type devices as well. Because the invention may be practiced in a variety of ways, the scope of the invention is only limited by the claims which now follow.

We claim:

1. A switchable semiconductor power device of the type which controls current conduction based on field effect principles, comprising:

a semiconductor layer having a transistor region including a source/drain formation and a termination region surrounding the transistor region, said termination region including an outer periphery corresponding to an edge of the device; and

a single conductor, configured for connection to a gate voltage supply, including first and second conductor portions with the first conductor portion formed in a trench and being positioned in the transistor region to control current flow through the source/drain formation and the second conductor portion positioned in the termination region, the second conductor portion: including a contact for connection to the gate voltage supply; and

including a feed comprising conductive material formed in a trench extending along the outer periphery and around the transistor region, said feed electrically connecting the contact with the first conductor portion; and acting as a field plate to extend the device breakdown voltage in the termination region; and

an isolation trench extending into the semiconductor layer and positioned between the edge of the device and the second conductor portion.

2. The device of claim 1 further comprising a plurality of additional source/drain formations each configured with the first conductor portion in and about a trench region to provide a voltage-switchable conduction channel for controlling current flow through the semiconductor layer.

3. The device of claim 1 wherein the transistor region comprises a vertical MOSFET device.

4. A method for manufacturing a semiconductor device, comprising:

providing on a layer of semiconductor material an active region and a termination periphery region surrounding the active region with a trenched transistor formation in the active region;

forming a trenched gate runner in the termination region along the active region; and

forming first and second conductor regions such that said first and second conductor regions are electrically connected to form a continuous conductor with multiple regions and said first conductor region is in said trenched transistor formation and said second conductor region is said trenched gate runner such that said second conductor also acts as a field plate termination; wherein

the trenched gate runner extends further into the layer of semiconductor material than the trenched transistor formation.

5. A method for manufacturing a semiconductor device, comprising:

US 6,818,947 B2

7

providing on a layer of semiconductor material an active region and a termination periphery region surrounding the active region with a trenched transistor formation in the active region;

forming a trenched gate runner in the termination region 5
along the active region, the trenched transistor formation including a gate conductor formed simultaneously with the gate runner by deposition of polysilicon; and

forming first and second conductor regions such that said first and second conductor regions are electrically connected to form a continuous conductor with multiple regions and said first conductor region is in said trenched transistor formation and said second conductor region is said trenched gate runner such that said second conductor also acts as a field plate termination 10 15

the trenched transistor formation including a gate conductor formed simultaneously with the gate runner by deposition of polysilicon

6. A semiconductor structure comprising:

a layer of semiconductor material having an active device region and a peripheral region surrounding the active region; 20

a transistor device formed in the active region including a plurality of source regions on one surface and drain region on the opposite surface; 25

8

a trench having an outer annular portion disposed in the peripheral region and enclosing the transistor device, the walls and the floor of the outer annular portion lined with an insulator and the outer annular portion filled with conductive material for forming a field plate around the transistor regions; and

a plurality of elongated inner runners extending in the same direction across the one surface with the source regions and intersecting the outer annular portion at opposite ends of the runners, the runners having their floors and their walls lined with a gate insulating material and the runners filled with a conductor

to form a gate structure in the transistor region to control current between the source regions and the drain.

7. The semiconductor of claim **6**, wherein the conductor material comprises conductive polysilicon.

8. The semiconductor of claim **7**, further comprising a layer of metal on the conductive polysilicon.

9. The semiconductor of claim **7** wherein the insulator in the outer annular portion is thicker than the gate insulator in the runners.

10. The semiconductor of claim **7** wherein a common layer of conductive polysilicon fills the trench.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,818,947 B2
DATED : November 16, 2004
INVENTOR(S) : Thomas E. Grebs et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1,

Line 55, replace "trenched" with -- trenches --

Column 2,

Lines 62 and 64, replace "to" with -- top --

Column 4,

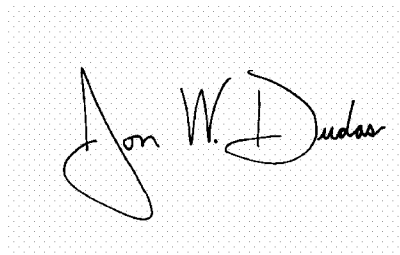
Line 64, replace "are had" with -- can be used --

Column 5,

Line 36, replace "ton" with -- top --

Signed and Sealed this

Twenty-ninth Day of March, 2005

A handwritten signature in black ink on a light gray dotted background. The signature reads "Jon W. Dudas" in a cursive, stylized script. The "J" is large and loops around the "on". The "W" is written with two distinct peaks. The "D" is large and loops around the "udas".

JON W. DUDAS

Director of the United States Patent and Trademark Office